Eiffel238i-2 Schematics Document

BOM Configuration
(R_):Unmount
(O_):OCP
(NONOCP_):NONOCP
(DBG_):Debug

Project code :3PD0CW010001
PCB No : 18449
Revision :-1
Project Name :EIFFEL238i-2
Size :264.0mm x 105.3mm

<Variant Name>

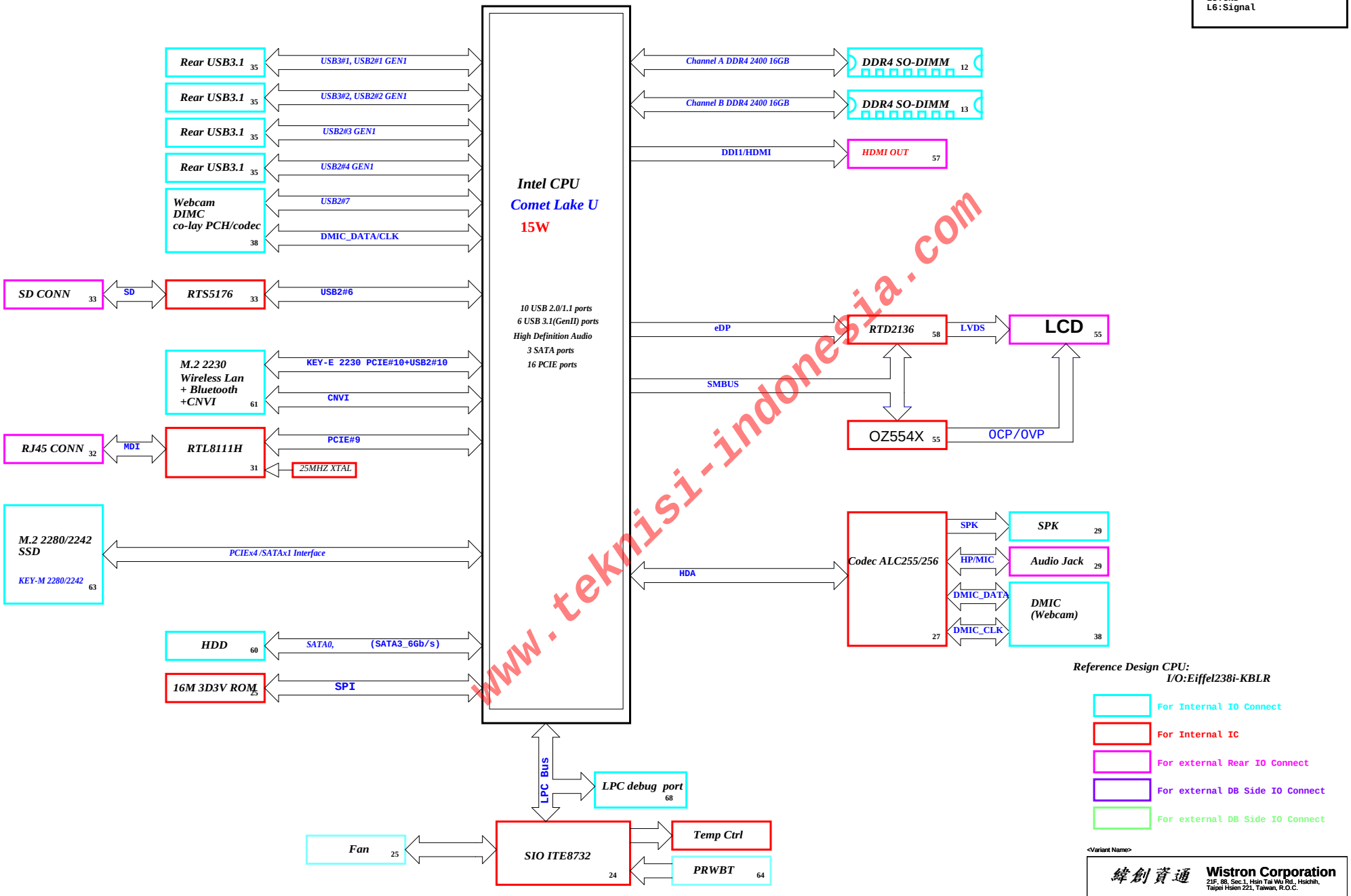
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page
Size: C | Document Number: Eiffel-2 | Rev: -1
Date: Thursday, June 27, 2019 | Sheet 1 of 106

Eiffel238i-2_CML Block Diagram

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal



Reference Design CPU:
I/O:Eiffel238i-KBLR

For Internal IO Connect
For Internal IC
For external Rear IO Connect
For external DB Side IO Connect
For external DB Side IO Connect

<Variant Name>

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Title: **Block Diagram**

Size	Document Number	Rev
C	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 2 of 106

SSID = CPU

PECI_EC
PROCHOT_N_EC

PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
XDP_TRST#
XDP_TCK_JTAGX

PROCHOT#_CPU_R

PROCHOT_N_OCP

BPM_CPU_N0
BPM_CPU_N1

XDP_PREQ#
XDP_PRDY#

1V_VCCST

1V_VCCSTG

20180528 SB Remove R310

Follow Aurora27_kblu
Damon SA Modify 10/26

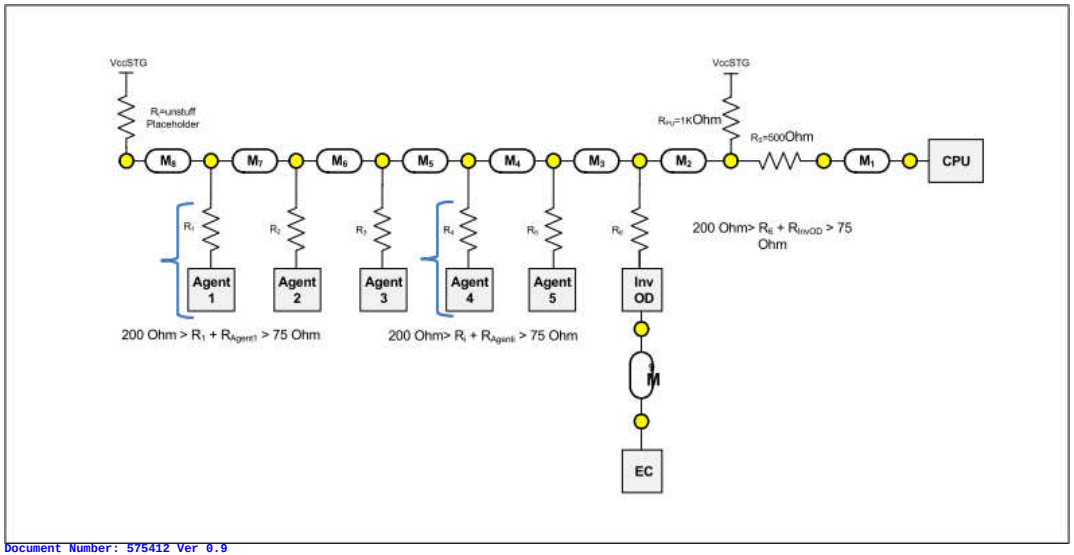
1V_VCCSTG

R307 1 2
499R2F-2-GP

R325(R_)
1 2
0R2J-2-GP

2017/05/02
Q2201 change to 84.T3904.H11/symbol 84.T3904.C11 obs

Add PROCHOT_N_EC Level shift Circuits,follow Eiffel215i_kulu
Damon SA Modify 10/30



Document Number: 575412 Ver 0.9

<Variant Name>

緯創資通 Wistron Corporation
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Title: CPU (THML/JTAG)

Size: A3 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 3 of 106

SSID = CPU

1 OF 20

eDP

eDP_TX_CPU_N0 56
eDP_TX_CPU_P0 56
eDP_TX_CPU_N1 56
eDP_TX_CPU_P1 56

eDP_AUX_CPU_N 56
eDP_AUX_CPU_P 56

eDP_HPD_CPU 56

eDP_BLEN_CPU 55
eDP_VDDEN_CPU 55
eDP_BLCTRL_CPU 55,56

HDMI

HDMI_DDI_TX_N0 57
HDMI_DDI_TX_P0 57
HDMI_DDI_TX_N1 57
HDMI_DDI_TX_P1 57
HDMI_DDI_TX_N2 57
HDMI_DDI_TX_P2 57
HDMI_DDI_TX_N3 57
HDMI_DDI_TX_P3 57

HDMI_SCL_CPU 57
HDMI_SDA_CPU 57

HDMI_DET_CPU 57

GPP_E23_STRAP 15
GPP_H17_STRAP 15

EC_SMI# 24

DP_SCL_CPU 15
DP_SDA_CPU 15

HDMI_DDI_TX_N2
HDMI_DDI_TX_P2
HDMI_DDI_TX_N1
HDMI_DDI_TX_P1
HDMI_DDI_TX_N0
HDMI_DDI_TX_P0
HDMI_DDI_TX_N3
HDMI_DDI_TX_P3

1V_VCCIO

R406_1 — 2 — eDP_RCOMP_CPU
24D9R2F-L-GP

HDMI_SCL_CPU
HDMI_SDA_CPU

DP_SCL_CPU
DP_SDA_CPU

GPP_E23_STRAP — Strap

GPP_H17_STRAP — Strap

eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1

eDP_AUX_CPU_N
eDP_AUX_CPU_P

HDMI_DET_CPU
EC_SMI#
EC_SCI#
eDP_HPD_CPU

eDP_BLEN_CPU
eDP_VDDEN_CPU
eDP_BLCTRL_CPU

3D3V_S5

EC_SMI# — R402_1 — 2 — 10KR2F-L1-GP (64.10025.6DL)
EC_SCI#

eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω ±1%	600 mils
Note: Must maintain low DC resistance routing (<0.1Ω)				

Document Number: 575412 Ver 0.9

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

Document Number: 575412 Ver 0.9 (Schematic Checklist)

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **CPU (DDI/EDP)**

Size: A3 | Document Number: **Eiffel-2** | Rev: **-1**

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SSID = CPU

DDR4 ball type: Interleaved Type

Document Number: 575414 Ver 1.2

NIL
IL
DDR4

M_A_DQS_DN0 12
M_A_DQS_DP0 12
M_A_DQS_DN1 12
M_A_DQS_DP1 12
M_A_DQS_DN2 12
M_A_DQS_DP2 12
M_A_DQS_DN3 12
M_A_DQS_DP3 12
M_A_DQS_DN4 12
M_A_DQS_DP4 12
M_A_DQS_DN5 12
M_A_DQS_DP5 12
M_A_DQS_DN6 12
M_A_DQS_DP6 12
M_A_DQS_DN7 12
M_A_DQS_DP7 12

M_B_DQS_DN0 13
M_B_DQS_DP0 13
M_B_DQS_DN1 13
M_B_DQS_DP1 13
M_B_DQS_DN2 13
M_B_DQS_DP2 13
M_B_DQS_DN3 13
M_B_DQS_DP3 13
M_B_DQS_DN4 13
M_B_DQS_DP4 13
M_B_DQS_DN5 13
M_B_DQS_DP5 13
M_B_DQS_DN6 13
M_B_DQS_DP6 13
M_B_DQS_DN7 13
M_B_DQS_DP7 13

M_A_DQ0 12
M_A_DQ1 12
M_A_DQ2 12
M_A_DQ3 12
M_A_DQ4 12
M_A_DQ5 12
M_A_DQ6 12
M_A_DQ7 12
M_A_DQ8 12
M_A_DQ9 12
M_A_DQ10 12
M_A_DQ11 12
M_A_DQ12 12
M_A_DQ13 12
M_A_DQ14 12
M_A_DQ15 12
M_A_DQ16 12
M_A_DQ17 12
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M_B_DQ0 13
M_B_DQ1 13
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M_B_DQ62 13
M_B_DQ63 13

M_A_CLK#1 12
M_A_CLK1 12
M_A_CLK#0 12
M_A_CLK0 12

M_A_CKE0 12
M_A_CKE1 12
M_A_CS#0 12
M_A_CS#1 12
M_A_ODT0 12
M_A_ODT1 12
M_A_A0 12
M_A_A1 12
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M_A_A8 12
M_A_A9 12
M_A_A10 12
M_A_A11 12
M_A_A12 12
M_A_A13 12
M_A_A14 12
M_A_A15 12
M_A_A16 12

M_A_ACT_N 12

M_A_BG0 12
M_A_BG1 12

M_A_BA0 12
M_A_BA1 12

M_A_ALERT_N 12

M_A_PARITY 12

V_SMA_VREF_CA 12
V_SMB_VREF_CA 13

SM_DRAMRST# 12,13

SM_PGCNTL 40

M_B_CLK#0 13
M_B_CLK0 13
M_B_CLK#1 13
M_B_CLK1 13

M_B_CKE0 13
M_B_CKE1 13

M_B_CS#0 13
M_B_CS#1 13

M_B_ODT0 13
M_B_ODT1 13

M_B_A0 13
M_B_A1 13
M_B_A2 13
M_B_A3 13
M_B_A4 13
M_B_A5 13
M_B_A6 13
M_B_A7 13
M_B_A8 13
M_B_A9 13
M_B_A10 13
M_B_A11 13
M_B_A12 13
M_B_A13 13
M_B_A14 13
M_B_A15 13
M_B_A16 13

M_B_ACT_N 13

M_B_BG0 13
M_B_BG1 13

M_B_BA0 13
M_B_BA1 13

M_B_ALERT_N 13

M_B_PARITY 13

M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

20180619 SB Add R508, R509

20180705 1 short pin

M_B_DQ[0:7]
M_B_DQ[8:15]
M_B_DQ[16:23]
M_B_DQ[24:31]
M_B_DQ[32:39]
M_B_DQ[40:47]
M_B_DQ[48:55]
M_B_DQ[56:63]

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

1D2V_S3

R505 1 2 121R2F-GP
R507 1 2 100R2F-L1-GP-U

20180705 1 short pin

Change to 1000pF
Damon SA Modify 10/31

<Variant Name>

緯創資通 Wistron Corporation
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Title: CPU (DDR)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

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SSID = CPU

CFG3
CFG4

15,99
15,99

CFG[19:0]

15,99

99

ITP_PMODE

Strap

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.

Document Number: 575418 Ver 1.1

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		
CFG[1]	Reserved. No connect			
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation 0 = Lane numbers reserved		
CFG[3]	Reserved configuration lane			
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1	
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*		
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.	1	
CFG[19:8]	Reserved configuration lands.			

Document Number: 575412 Ver 0.9 (Schematic Checklist)

<Variant Name>

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Title: CPU (CFG/IST)

Size: A3 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 6 of 106

PWR_VCC_SENSE
PWR_VSS_SENSE

SVID_ALERT#_CPU
SVID_CLK_CPU
SVID_DATA_CPU

SSID = CPU

46
46

1V_CPU_CORE
46
46
46

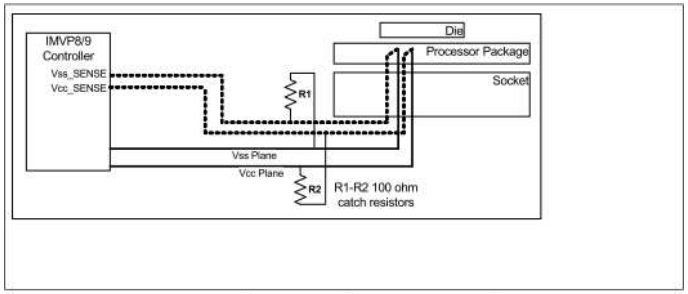
1V_CPU_CORE

1V_CPU_CORE

R1

R2

R702
100R2F-L1-GP-U



Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
	100Ω	50Ω	<25 mils
Vcc_SENSE /Vss_SENSE			
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Document Number: 575412 Ver 0.9

Document Number: 575418 Ver 1.1
Vcc 70A(Max)

1V_VCCST

SVID ALERT

1V_VCCSTG

SVID CLOCK

1V_VCCST

change to 43R,follow CRB
Damon SA Modify 11/01

1V_VCCIO

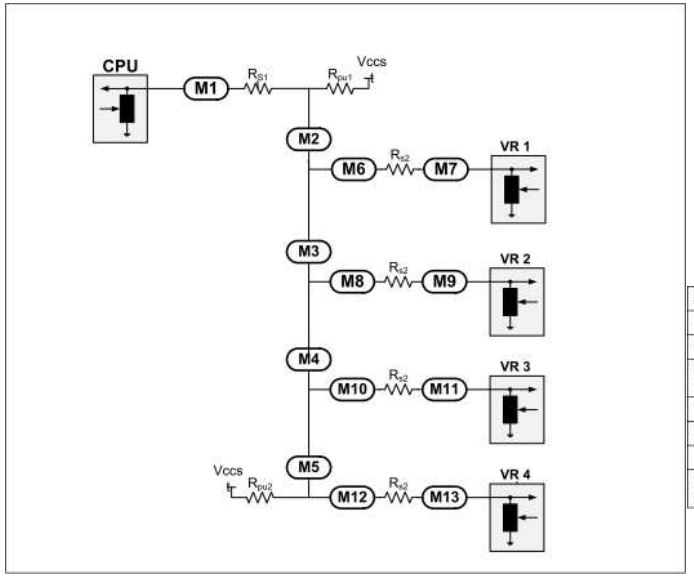
1V_VCCSTG

Follow Eiffel215i_KblU
Damon SA Modify 10/29

C710 (R_)
SC1U10V2KX-L1GP
Near R709
Damon 03/28

20180705 1 short pin
1V_VCCST

SVID DATA



SVID Signals	VIDSOUT, VIDSCK, VIDSALERT# 20180705 1 short pin
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

<Variant Name>

緯創資通 Wistron Corporation
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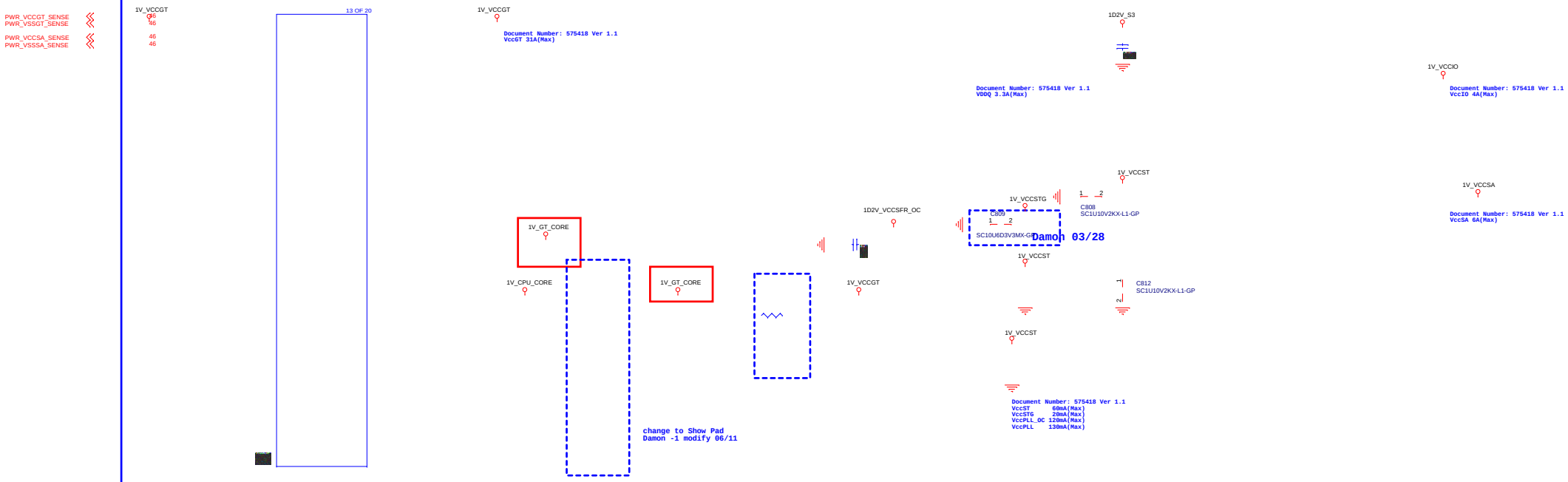
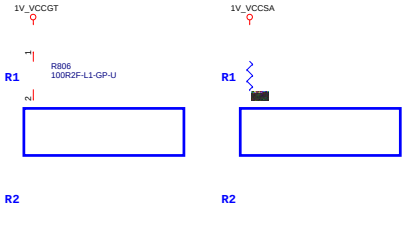
Title: CPU (VCORE/VID)
Size: Custom | Document Number: Eiffel-2 | Rev: -1
Date: Thursday, June 27, 2019 | Sheet 7 of 106



Date	Revision	Description		
		Ball#	Old Name	New Name
01/Nov/2017	1.0	Initial revision	Initial revision	Initial revision
22/Dec/2017	1.1	AA9, AB10, AB2, AB8, AB9, AC8, AD9, AE10, AE8, AE9, AF10, AF2, AF8, AG8, AG9, AH9, AJ10, AJ8, AK2, AK9, AL10, AL8, AL9, AM8, V2, Y10, Y8	VCCGT	VCCCORE
	1.2	AL1	IST_TP[1]	RSVD
		AL2	IST_TP[0]	RSVD
		AL3	IST_TRIG[1]	RSVD
		AL4	IST_TRIG[0]	RSVD
		AM3, AT3, AU3, BJ34, BJ36, BP8, BP9, BT8, BT9, CR35	RSVD_TP	RSVD
		CF25	GPP_H21	GPP_H21 / XTAL_FREQ_SELECT

Document Number: 575414 Ver 1.2



R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
Vcc_{GT}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*

Document Number: 575412 Ver 0.9

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VCCGT/VCCIO/VDDQ/VCCSA)

Size: A2 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 8 of 106

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (RSVD)	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 9 of 106	

Main Func = CPU

VCORE

WHL_U42

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	35	330uF*2

1V_CPU_CORE

PC1002 PC1004 PC1005 PC1007 PC1008 PC1009 PC1010 PC1013 PC1016 PC1020 PC1021 PC1023 PC1024 PC1027 PC1029 PC1034 PC1036 PC1038 PC1039 PC1042 PC1043 PC1044 PC1045 PC1046

VCCGT

WHL_U42

U42
IccMax current-10ms max = 31 A

22uF	PCS	Cap
RT	26	330uF*1

1V_VCCGT

DY

PC1048 PC1049 PC1050 PC1052 PC1055 PC1056 PC1061 PC1062 PC1066 PC1068 PC1069 PC1070 PC1073 PC1076

VCCSA

WHL_U42

U42
IccMax current-10ms max = 5 A

22uF	PCS
RT	8

1V_VCCSA

PC1084 PC1085 PC1086 PC1089 PC1091

GT_CORE

1V_GT_CORE

PC1079 PC1080 PC1083

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_(Power CAP1)*

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 10 of 106

SSID = PCH

1D2V_S3

20180614 SB Add 10 pcs cap reserve

1D0V_S5

C1112 SC22U6D3V3MX-L1-GP

C1128 SC22U6D3V3MX-L1-GP

C1129 SC22U6D3V3MX-L1-GP

C1153 SC10U6D3V3MX-GP

(R_) C1154 SC10U6D3V3MX-GP

(R_) C1161 SC10U6D3V3MX-GP

1D0V_S5

1D05V_VCCPRIM

20180705 1 short pin

20180705 1 short pin

3D3V_S5

3D3V_VCCPRIM

R1103 0R0603-PAD-1-GP-U

20180705 1 short pin

C1113 SC22U6D3V3MX-L1-GP (R_)

3D3V_VCCPRIM

C1123 SC10U6D3V3MX-L-GP (R_78:10610.5BL)

1D8V_S5

R1104 0R0603-PAD-1-GP-U

20180705 1 short pin

1D8V_VCCPRIM

1D0V_S5

1D0V_VCCPRIM_CORE

R1105 0R0603-PAD-1-GP-U

20180705 1 short pin

R1106 0R0603-PAD-1-GP-U

20180705 1 short pin

20180705 1 short pin

20180705 1 short pin

1D2V_S3

(R_) C1136 SC10U6D3V3MX-GP

C1137 SC10U6D3V3MX-GP

C1138 SC10U6D3V3MX-GP

C1132 SC22U6D3V3MX-L1-GP

C1145 SC1U10V2KX-L1-GP

C1146 SC1U10V2KX-L1-GP

1V_VCCIO

1V_VCCIO

(R_) C1135 SC22U6D3V3MX-L1-GP

C1111 SC1U10V2KX-L1-GP

C1149 SC1U10V2KX-L1-GP

(R_) C1150 SC1U10V2KX-L1-GP

C1152 SC1U10V2KX-L1-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power Cap2)

Size: A4 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 11 of 106

SSID = DDR4 CHA

Please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

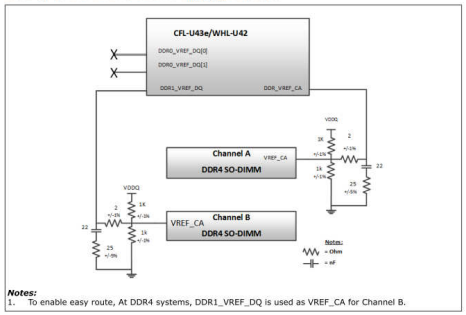
H=8mm

need close to PIN 255

Swap modify with Layout
Damon Wei SA 11/03

Thermal EVENT

Figure 4-1. WHL-U/CFL-U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Figure 4-2. WHL-U/CFL-U DDR4 SODIMM T3/8L Inline SBS NIL Placement and Block Diagram

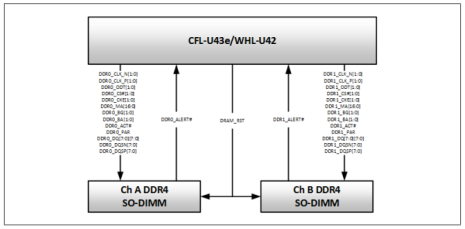


Figure 4-3. WHL-U/CFL-U DDR4 SODIMM T3/8L B2B IL Placement and Block Diagram

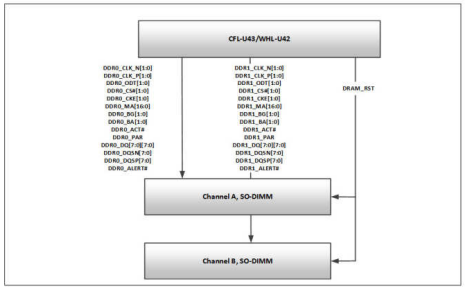
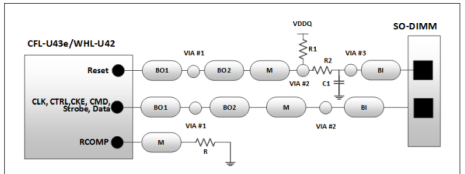


Figure 4-4. WHL-U/CFL-U DDR4 SODIMM T3/8L Signals Topologies



Note: DRAM_RST C1 capacitor should not be installed

<Variant Name>
緯創資通 Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4_CHA)

Size	Document Number	Rev
D	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 12 of 186

SSID = DDR4 CHB

Note:
SO-DIMMB SPD Address is 0xA4

H=4mm

need close to PIN 255

3D3V_S0
C1338 SCD1U16V2KX-L-GP
C1339 SC2D2U10V3KX-L-GP (78.22523.5BL)
(R_)

1D2V_S3
3 OF 4
2D5V_S3
0D6V_VREF_S0

DQS1 DQ8~DQ15
DQS0 DQ0~DQ7
DQS2 DQ16~DQ23
DQS3 DQ24~DQ31
4 OF 4
DQS4 DQ32~DQ39
DQS5 DQ40~DQ47
DQS6 DQ48~DQ55
DQS7 DQ56~DQ63

SPD Address of DIMM1

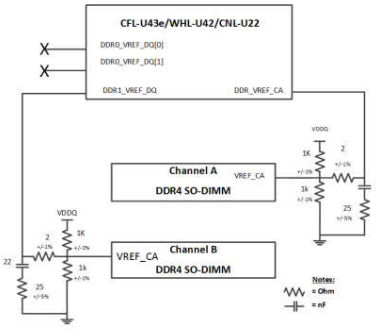
SPD SA1	1
SPD SA0	0

3D3V_S0

M_VREF_CA_DIMMB

Thermal EVENT

1D2V_S3



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

1D2V_S3
M_VREF_CA_DIMMB
C1302 SCD1U16V2KX-L-GP (78.10421.2FL)

Layout Note:

Signal Group	Segment	Routing Layer	Max Length (mils) Segment	Max Length (mils) Total (PKG+MB)	Target Zse (ohm)	Target Zdiff (ohm)	Trace Width, W (mils)	Trace Spacing, S1 (mils): Within Group	Trace Spacing, S2 (mils): CMD/CTRL/CLK to DQ/DQS	Trace Spacing, S3 (mils): Byte to Byte	Trace Spacing (mil), Within DIFF pair	Trace Spacing (mil), DQS pair to DQ	Trace Spacing (mil), CLK pair to CMD/CTRL/ CKE	Ct/Rtt
Vref	M	SL					20	10	20					Refer to Fig.
RCOMP (0/1/2)	M	US/SL	500				15	20	25					CFL-U43e/ WHL-U42: 121/80.6/ 100 CNL-U22: 100/100/ 100

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to SODIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to SODIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)
		Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

Place these Caps near DIMM1.

1D2V_S3
C1313 SCD10U6D3VMX-L-GP (78.10610.58L)
C1329 SCD10U6D3VMX-L-GP (78.10610.58L)
C1331 SCD1U10V2KX-L-GP
C1333 SCD1U10V2KX-L-GP
C1334 SCD1U10V2KX-L-GP
C1336 SCD1U10V2KX-L-GP

2D5V_S3
C1342 SCD10U6D3VMX-L-GP (78.10610.58L)
C1343 SCD10U6D3VMX-L-GP
0D6V_VREF_S0
(R_)
C1321 SCD10U6D3VMX-L-GP
C1319 SCD1U10V2KX-L-GP

Document Number: 575412 Ver 0.9

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4_CHB)
Size: A2 | Document Number: Eiffel-2 | Rev: -1
Date: Thursday, June 27, 2019 | Sheet 13 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

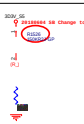
Title: DDR (RSVD)

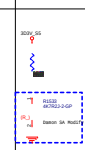
Size	Document Number	Rev
D	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 14 of 186

Main Func = PCH

Description	Top Swap Override	No Reboot	TLS Confi-dentiality	Boot BIOS Strap Bit BBS	eSPI or LPC
GPIO	GPP_B14	GPP_B18	GPP_C2	GPP_B22	GPP_C5
Schematics					
High	Enable	Enable	Enable	LPC	eSPI
Low	Disable	Disable	Disable	SPI	LPC
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Reserved	Reserved	IntelR DCI-OOB	Reserved	Reserved
GPIO	SPI0_MOSI	GPP_D12	GPP_B23	SPI0_IO2	SPI0_IO3
Schematics					
High			Enable		
Low			Disable		
			internal pull-down		

Description	Flash Descriptor Security Override	Display Port B Detected	Display Port C Detected	Display Port D Detected	Reserved
GPIO	HDA_SDO	GPP_E19	GPP_E21	GPP_E23	GPP_H17
Schematics		Page.004	Page.004	Page.004 	
High	Disable	Detected	Detected	Detected	
Low	Enable	not detected	not detected	not detected	
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	XTAL Frequency Select	M.2 CNV Mode Select	3.0V Select	Reserved	eSPI Flash Sharing Mode
GPIO	GPP_H21	GPP_F6	INPUT3VSEL	GPD7	GPP_H23
Schematics					
High	24 MHz	Disable	3.0V +/- 5%		(SAFS) enabled
Low	38.4 MHz	Enable	3.3V +/- 5%		(MAFS) enabled
	internal pull-down				internal pull-down

CFG:

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and Firmware Hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. This is used to recover from a bad boot block. The size of two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) are selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). **Notes:** 1. "the internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system has booted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DC8, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. "the internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination Bit (Bus0, Device31, Function0, offset DC8, bit 6). **Bit 6 / Boot BIOS Destination** 0 / SPI (Default) 1 / LPC **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SMLBALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning:** **If this strap is configured to '0' (eSPI Flash Sharing Mode = SAFS), Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)**

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_D12 / IBH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SMLALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default). 1 = Enable Intel® DCI-OOB **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

HDA_SDO / I2S2_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / GSPI0_CTRLDATA / CNV_BT_IF_SELEC T	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / GSPI1_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port D is not detected. [Default] 1 = Port D is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL Frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	A weak external pull-up is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. **Note:** When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down is disabled. We pull this strap road to enable CNVi interface.
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required. 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% **Note:** This strap should only be used for specific targeted S3 battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default). 1 = Slave Attached Flash Sharing (SAFS) enabled. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning:** **This strap must be configured to '0' (eSPI Flash Sharing Mode = SAFS) if LPC or eSPI strap is configured to '0' (eSPI is disabled)**

<Variant Name>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
Custom	Eiffel-2	-1

Date: Wednesday, June 23, 2010 Sheet 6 of 108

SSID= PCH

Document Number: 575412 Ver 0.9
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

M.2 PCIE SSD1

SSD1_PCIE_RX_N3 63
SSD1_PCIE_RX_P3 63
SSD1_PCIE_TX_N3 63
SSD1_PCIE_TX_P3 63
SSD1_PCIE_RX_N2 63
SSD1_PCIE_RX_P2 63
SSD1_PCIE_TX_N2 63
SSD1_PCIE_TX_P2 63

SSD1_PCIE_RX_N1 63
SSD1_PCIE_RX_P1 63
SSD1_PCIE_TX_N1 63
SSD1_PCIE_TX_P1 63
SSD1_PCIE_RX_N0 63
SSD1_PCIE_RX_P0 63
SSD1_PCIE_TX_N0 63
SSD1_PCIE_TX_P0 63

WLAN

WLAN_PCIE_RX_N 61
WLAN_PCIE_RX_P 61
WLAN_PCIE_TX_N_C 61
WLAN_PCIE_TX_P_C 61

HDD

HDD_SATA_RX_N 60
HDD_SATA_RX_P 60
HDD_SATA_TX_N 60
HDD_SATA_TX_P 60

USB3 port1

BT_USB20_N 61
BT_USB20_P 61

CCD_USB20_N 30
CCD_USB20_P 30

CR_USB20_N 33
CR_USB20_P 33

DEVSLP2 63

USB3 port2

USB1_USB30_RX_N 35
USB1_USB30_RX_P 35
USB1_USB30_TX_N 35
USB1_USB30_TX_P 35

USB1_USB20_N 35
USB1_USB20_P 35

USB3 port3

USB2_USB30_RX_N 35
USB2_USB30_RX_P 35
USB2_USB30_TX_N 35
USB2_USB30_TX_P 35

USB2_USB20_N 35
USB2_USB20_P 35

USB3 port4

USB3_USB30_RX_N 34
USB3_USB30_RX_P 34
USB3_USB30_TX_N 34
USB3_USB30_TX_P 34

USB3_USB20_N 34
USB3_USB20_P 34

LAN

USB4_USB30_RX_N 34
USB4_USB30_RX_P 34
USB4_USB30_TX_N 34
USB4_USB30_TX_P 34

USB4_USB20_N 34
USB4_USB20_P 34

LAN_PCIE_RX_N_C 31
LAN_PCIE_RX_P_C 31
LAN_PCIE_TX_N_C 31
LAN_PCIE_TX_P_C 31

HPGP_M2_SATA_DET# 63

LAN

WLAN

HDD

M.2 PCIE SSD1

Add to Lan
Damon 2018/10/18 SA

Add to PCIEx4, support X4 Optane
Damon SA Modify 2018/10/25

USB3R1(USB 3.0)

USB3R2(USB 3.0)

USB3R3(USB 3.0)

USB3R4(USB 3.0)

USB3R1(USB 2.0)
USB3R2(USB 2.0)
USB3R3(USB 2.0)
USB3R4(USB 2.0)

Card Read
Camera

BT

20180613 SB Modify

3D3V_S0

3D3V_S0

3D3V_S5

EC1601
SCD1U25V2KX-L-GP
Document Number: 575412 Ver 0.9
EMC Sensitive Nets

M.2 auto detection
H:PCIE
L:SATA

3D3V_S5

1 R1608 2
10KR2J-3-GP

Change PH to 3D3V_S5
Damon SB modify 01/21

HSIO Lane Assignments – Comet Lake U PCH-LP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
USB3.1/3.0 #1	USB3.1/3.0 #2	USB3.1/3.0 #3	USB3.1/3.0 #4	USB3.1/3.0 #5	USB3.1/3.0 #6	PCIe 3.0 #7	PCIe 3.0 #8	PCIe 3.0 #9	PCIe 3.0 #10	PCIe 3.0 #11	PCIe 3.0 #12	PCIe 3.0 #13	PCIe 3.0 #14	PCIe 3.0 #15	PCIe 3.0 #16
PCIe 3.0 #1	PCIe 3.0 #2	PCIe 3.0 #3	PCIe 3.0 #4	PCIe G.0#5	PCIe 3.0 #6	GbE (LAN)	GbE (LAN)	GbE (LAN)		SATA #0	SATA #1	GbE (LAN)	GbE (LAN)	SATA #1**	SATA #2
PCIe X4				PCIe X4				PCIe X4				PCIe X4			
X2		X2		X2		X2		X2		X2		X2			
No Remapping								Intel® RST for PCIe Storage				Intel® RST for PCIe Storage			

** SATA P1 can be configured to PCIe Port 12 or 15.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium U	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	PCIe LAN	PCIe LAN	PCIe LAN	PCIe	PCIe SATA	PCIe SATA	PCIe LAN	PCIe LAN	PCIe SATA	PCIe SATA
Premium Y	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	USB3.1 PCIe	PCIe LAN	PCIe LAN	PCIe LAN	PCIe	PCIe SATA	PCIe SATA	PCIe LAN	PCIe LAN		
Mainstream U	USB3.0	USB3.0	USB3.0	USB3.0	PCIe	PCIe	PCIe LAN	PCIe LAN	PCIe LAN	PCIe	PCIe SATA	PCIe SATA	PCIe LAN	PCIe LAN	PCIe	PCIe

Intel® RST for PCIe Storage port configurable as M.2 x2/x4

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

6.4.5 PCH PCI Express* Impedance Compensation Guidelines

Figure 6-6. PCH PCIE_RCOMPP and PCIE_RCOMPN Connections

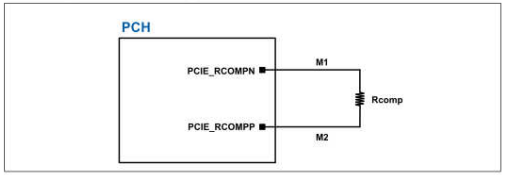


Table 6-10. PCH PCI Express* Compensation Routing Guidelines

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	M1, M2	MS/SL/DSL	NA	GND	GND	GND
Series Resistor	M1, M2	MS	Ohms	100 +/-1%	100 +/-1%	100 +/-1%
Motherboard Max Via Count	M1, M2	NA	vias	2	2	2
Motherboard Length Matching	M1, M2	MS/SL/DSL	mm(mils)	M1- M2 = ± 0.127mm (± 5mils)		

Notes:
1. Recommended placing a VSS shield of at least 4mils (0.1016mm) wide between the RCOMP signals and any adjacent I/O signal
2. Avoid routing close to any clocks
3. Micro-Vias within the breakout area are not counted against maximum via total
4. Must maintain low DC resistance routing (<0.1 ohm)

Document Number: 575412 Ver 0.9

CNVi:

Bluetooth USB host bus (positive) for standard CNV. Optional to connect to a Bluetooth USB+ pin on the Bluetooth module. Port 10 is the recommended port but other USB2 ports can be selected for this function.

Document Number: 566439 Ver 2.0

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/SATA/USB)

Size: A2 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 16 of 106

SSID = PCH

PLT_RST# 34,21,69,69,99

ALL_SYS_PWRGD 40

SYS_PWROK 24,43,68,99

PCH_PWROK 40

PCIE_WAKE# 61,63

PM_SLP_S0# 40,52

PM_SLP_S3# 24,40,52,68

PM_SLP_S4# 24,34,40,52,68

PM_PWRBTN# 24,99

INPUT3VSEL 15

PM_SLP_SUSB# 24,52,53

PCH_DPWROK 24

LAN_WAKE# 31

VCCST_PWRGD 40,99

XDP_DBRESET# 99

EXT_PWR_GATE# 24

Damon 0409

Follow EIFFEL215I_KBLU
Damon SA Modify 10/30

2016/10/27 add follow CRB

Follow Aurora27_kblu
Damon SA Modify 10/26

Strap

ECIO_RSMRST# 24 99 PM_RSMRST#

Follow Eiffel215i_KBLU
2018/10/17 Damon Wei Modify

3D3V_S5

Follow Aurora27_kblu
Damon SA Modify 10/26

20180528 SB Remove RN1702, Add R1702, R1703

3D3V_S5

3D3V_S5

3D3V_RTC_AUX

Document Number: 576715 Ver 0.5
pull-up 330K

3D3V_S5

20180604 Change to DY

Document Number: 575412 Ver 0.9
EMC Sensitive Nets

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size: A3 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 17 of 106

SSID = PCH

SPI_CLK_ROM
SPI_SO_ROM
SPI_SI_ROM
SPI_WP_CPU
SPI_HOLD_CPU
SPI_WP_ROM
SPI_HOLD_ROM
SPI_CS_CPU_N0_R
SPI_SI_CPU

H_RCIN#
INT_SERIRQ

CPU_SMB_SDA_DDR
CPU_SMB_SCL_DDR

GPP_C2/SMBALERT#
GPP_C5/SML0ALERT#
GPP_B23/SML1ALERT#

LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
LPC_FRAME#_CPU

LPC_CLK_SIO_P0
LPC_CLK_DBG
CPU_SMB_SDA
CPU_SMB_SCL

PM_CLKRUN#_EC

SPI_WP_XDP

Damon 0409
Change to 49.9R,follow PDG.
Damon SA Modify 11/02

Strap
Strap
Strap
Strap

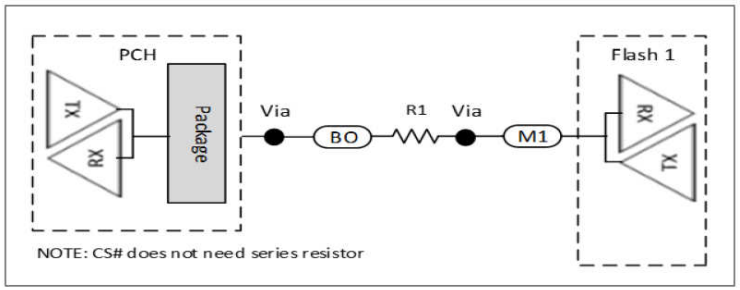
@S5 domain for TSMT1&WLAN
@S0 domain for DIMM1&DIMM2&XDP
No used
No used

GPI
Single-Ended 24-MHz output

20180528 SB Change to 3D3V_S0

3D3V_S0
3D3V_S0
3D3V_S5
3D3V_S5
3D3V_S0

). SPI0 Single Load Topology



20180604 SB Change to DY
Document Number: 575412 Ver 0.9
EMC Sensitive Nets

R1813 1 24 2 22R2J-2-GP LPC_CLK_SIO_P1

1823 Simon
add for EMI solution
Please close R1805

WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_CLKREQ_CPU#

SSD1_CLK_CPU_N
SSD1_CLK_CPU_P
SSD1_CLKREQ_CPU_N

PULSAR_38P4M_REFCLK
SUS_CLK_CPU

LAN_CLK_CPU_N_C
LAN_CLK_CPU_P_C
LAN_CLKREQ_CPU_N

XDP_CLK_CPU_N
XDP_CLK_CPU_P

RTC_RST#

Add Lan CLK and REQ
Damon 2018/10/18 SA

LAN
WLAN
NGFF1

3D3V_S0

R1907 move to PCH side

PULSAR_38P4M_REFCLK

20180705 1 short pin
R1813 EMC suggestion: 68.00084.921

ER1802
10KR2J-3-GP
CNVi

3D3V_RTC_AUX

20180615 SB Change C1807, C1808, R1841 value

20180607 SB Change C1803, C1804 value

RTC Reset

RTC Reset follow Eiffel215i_Kblu
Damon Wei SA Modify 2018/10/18

For AFR

RTCRST_ON

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(SPI/ESPI/SMBS/XTAL/CLK)
Size: Custom | Document Number: Eiffel-2 | Rev: -1
Date: Thursday, June 27, 2019 | Sheet 18 of 106

SSID = PCH

HDA_SYNC_CODEC 27
HDA_BITCLK_CODEC 27
HDA_SDOUT_CPU 15
HDA_SDOUT_CODEC 27

HDA_SDIN0_CPU 27

DMIC1_DATA_CPU 30
DMIC1_CLK_CPU 30

HDA_RST_N_CODEC 27
HDA_SPKR 15,27
BT_PCMFRM_RSTN 61
BT_PCMOUT_CLKREQ0 61

Strap

Strap

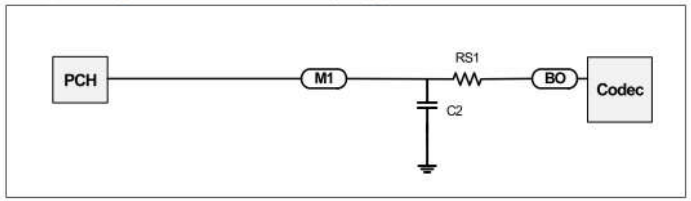
Close to PCH

SD_RCOMP:

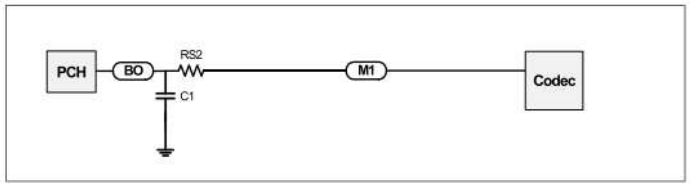
SD_3P3_RCOMP and SD_1P8_RCOMP precision resistors are still needed, even if SDXC interface is not used.

Document Number: 575412 Ver 2.0

HDA_SDI Single Load Audio Down Topology



HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Topology



Document Number: 575412 Ver 2.0

Add ME_CNTL Circuit,follow Eiffel215i_KBLU
2018/10/17 Damon Wei Modify

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Debug mode

3D3V_S5
R1915
1KR2J-1-GP

ME_UNLOCK 20

1. Resume GPIO
2. Default High

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HDA/I2S/SD/DMIC)
Size: Custom
Document Number: Eiffel-2
Rev: -1
Date: Thursday, June 27, 2019
Sheet 19 of 106

SSID = PCH

NRB_BIT
RTC_DET#
GPP_B22_GSPI1_MOSI
GPP_D12
CNV_BRI_RSP
CNV_RGI_DT
CNV_BRI_DT
CNV_RGI_RSP
LPC_PME#

15
25
15
15
61
15,61
61
61
24

PIRQA#
NRB_BIT
RTC_DET#
LPC_PME#
DGPU_PWR_EN#
GPP_B22_GSPI1_MOSI
CNV_BRI_RSP
CNV_RGI_DT_R
CNV_BRI_DT_R
CNV_RGI_RSP

TP2002
R2001 33R2J-2-GP
R2003 33R2J-2-GP

SMI/SCI PIN
THERMAL_SHUT#

3D3V_S0
R2041 10KR2F-2-GP (R_)

6 OF20
Strap
Strap
Strap
Strap

GPP_D12
HDD_PWR_EN
3D3V_S5
ME_UNLOCK
ME_UNLOCK
DGPU_HOLD_RST#

Change PH to 3D3V_S5
Damon SB modify 01/21
3D3V_S5
PIRQA#
R2053 1 (64.10025.6DL) 2 10KR2F-L1-GP
3D3V_S5
RTC_DET#

1D8V_S5
CNV_BRI_RSP
CNV_RGI_RSP
R2015 20KR2J-L2-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A2
Document Number: Eiffel-2
Rev: -1
Date: Thursday, June 27, 2019
Sheet 20 of 106

SSID = PCH

Primary Well Group F (1.8 V Only)

Document Number: 566439 Ver.2.0

CPU_C10_GATE# 24,49

GPP_H21 15

GPP_H23 15

GPD_7 15

CNV_WR_DN0
CNV_WR_DP0
CNV_WR_DN1
CNV_WR_DP1

CNV_WT_DN0
CNV_WT_DP0
CNV_WT_DN1
CNV_WT_DP1

CNV_WR_CLK_DN
CNV_WR_CLK_DP

CNV_WT_CLK_DN
CNV_WT_CLK_DP

CNV_WR_DN0 61
CNV_WR_DP0 61
CNV_WR_DN1 61
CNV_WR_DP1 61
CNV_WT_DN0 61
CNV_WT_DP0 61
CNV_WT_DN1 61
CNV_WT_DP1 61
CNV_WR_CLK_DN 61
CNV_WR_CLK_DP 61
CNV_WT_CLK_DN 61
CNV_WT_CLK_DP 61
CNV_WT_RCOMP

R2101
150R2F-1-GP

9 OF 20

Strap
Strap
Strap

Damon 0111

CPU_C10_GATE# → CPU_C10_GATE#_R

GPP_H21
GPP_H23
GPD_7

EMMC_RCOMP — R2108 1 — 2 200R2F-L-GP

Signal	Trace Width	Resistor Value	Isolation Spacing	Max Length
EMMC_RCOMP	M1: 0.10mm/4 mils min(breakout); typically 0.203-0.305mm/ 8-12 mils trace. Must maintain low DC resistance of <0.1 Ohm.	200 Ohm +/- 1% external resistor pull down to GND.	At least 0.308mm/12 mils to any adjacent I/O.	NA

Document Number: 575412 Ver 0.9

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

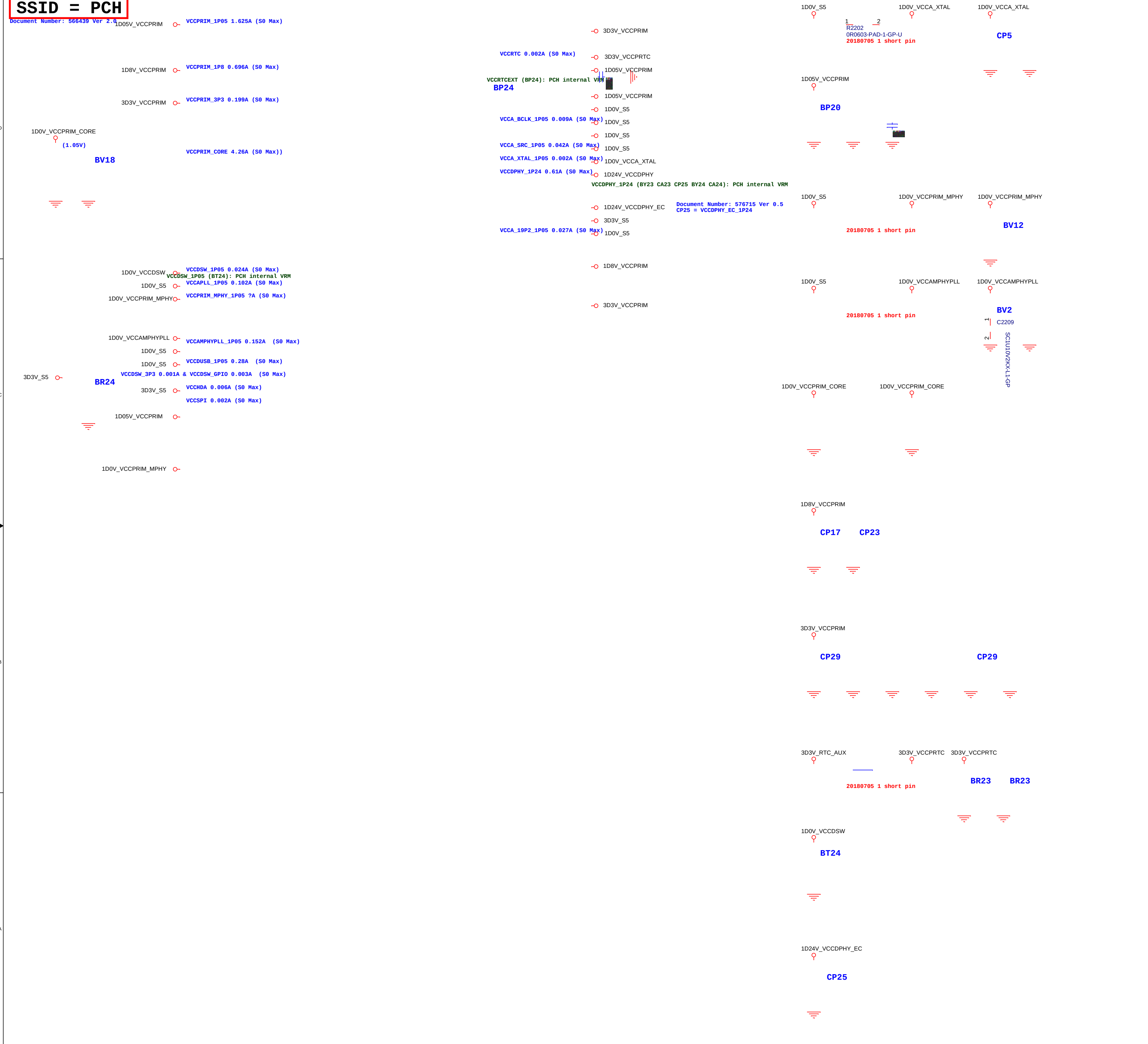
Title: CPU (EMMC/CNVi)

Size: A4 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 21 of 106

SSID = PCH

Document Number: 566439 Ver 2.0



1D05V_VCCPRIM
VCCPRIM_1P05 1.625A (S0 Max)
1D8V_VCCPRIM
VCCPRIM_1P8 0.696A (S0 Max)
3D3V_VCCPRIM
VCCPRIM_3P3 0.199A (S0 Max)
1D0V_VCCPRIM_CORE
(1.05V)
BV18
VCCPRIM_CORE 4.26A (S0 Max))
1D0V_VCCDSW
VCCDSW_1P05 0.024A (S0 Max)
VCCDSW_1P05 (BT24): PCH internal VRM
1D0V_S5
VCCAPLL_1P05 0.102A (S0 Max)
1D0V_VCCPRIM_MPHY
VCCPRIM_MPHY_1P05 ?A (S0 Max)
1D0V_VCCAMPHYPLL
VCCAMPHYPLL_1P05 0.152A (S0 Max)
1D0V_S5
1D0V_S5
VCCDUSB_1P05 0.28A (S0 Max)
3D3V_S5
BR24
VCCDSW_3P3 0.001A & VCCDSW_GPIO 0.003A (S0 Max)
3D3V_S5
VCCHDA 0.006A (S0 Max)
VCCSPI 0.002A (S0 Max)
1D05V_VCCPRIM
1D0V_VCCPRIM_MPHY
3D3V_VCCPRIM
VCCRTC 0.002A (S0 Max)
3D3V_VCCPRTC
VCCRTCEXT (BP24): PCH internal VRM
BP24
1D05V_VCCPRIM
1D05V_VCCPRIM
VCCA_BCLK_1P05 0.009A (S0 Max)
1D0V_S5
1D0V_S5
VCCA_SRC_1P05 0.042A (S0 Max)
1D0V_S5
1D0V_S5
VCCA_XTAL_1P05 0.002A (S0 Max)
1D0V_VCCA_XTAL
VCCDPHY_1P24 0.61A (S0 Max)
1D24V_VCCDPHY
VCCDPHY_1P24 (BY23 CA23 CP25 BY24 CA24): PCH internal VRM
1D24V_VCCDPHY_EC
Document Number: 576715 Ver 0.5
CP25 = VCCDPHY_EC_1P24
3D3V_S5
VCCA_19P2_1P05 0.027A (S0 Max)
1D0V_S5
1D8V_VCCPRIM
3D3V_VCCPRIM
1D0V_S5
1D0V_VCCA_XTAL
1D0V_VCCA_XTAL
R2202
0R0603-PAD-1-GP-U
20180705 1 short pin
CP5
1D05V_VCCPRIM
BP20
1D0V_S5
1D0V_VCCPRIM_MPHY
1D0V_VCCPRIM_MPHY
20180705 1 short pin
BV12
1D0V_S5
1D0V_VCCAMPHYPLL
1D0V_VCCAMPHYPLL
20180705 1 short pin
BV2
C2209
SC1U10V2KX-L1-GP
1D0V_VCCPRIM_CORE
1D0V_VCCPRIM_CORE
1D8V_VCCPRIM
CP17
CP23
3D3V_VCCPRIM
CP29
CP29
3D3V_RTC_AUX
3D3V_VCCPRTC
3D3V_VCCPRTC
20180705 1 short pin
BR23
BR23
1D0V_VCCDSW
BT24
1D24V_VCCDPHY_EC
CP25

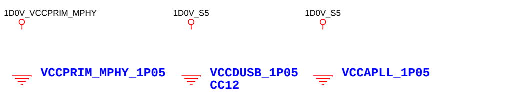
Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP22, BP20, BW16, BW18, BW19, BY16, CA14, BR20, BY20, BT18, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BY12, BY14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.05A / V0.75A	VCCPRIM_CORE	BU15, BU22, BV15, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23, CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29, BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BY24, CA24	4.7uF	0402	1	E	CP25

Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin CP5) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin BV2) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

Document Number: 575412 Ver 0.9

Document Number: 575412 Ver 0.9
EMC Sensitive Nets



<Variant Name>

SSID = PCH

17 OF 20

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (VSS)*

Size: A3 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 23 of 106

FAN

LPC

Power Manager

CLOCK

OTHERS

SMBUS

CONVERTOR SMB

HW Monitor

VRD

Layout Note: place it near CPU VORE MOS

REMINE LAYOUT

PCH

SYS

2014/8/20 add DIMM_TMPIN3 circuit

PCH Reset signals

IT8732 Power On Strapping Options

	Symbol	value	Description
JP1 Pin 60	DSW_EUP_SEL	1	EUP
		0	DSW

If without use these pins, Please pull-up to 3.3V. Don't let it floating
Pin19/24/25/36/48/57/71/75/77/80-83/86/95

SM Bus PH
SMB_DATA/CLK

COM port

Print port

GPO

For Power monitor function

Case Open Detection

Note: COPEN# should be connected to GND when this function is not be used.

EC control pin for CNVBD2

LPC I/F

Debug

For AC OFF SEQUENCE

SPI Interface

1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash

change to 1Mbit

072.25010.0A01

Del C2450 Vendor advice
Damon SA Modify 11/29

For EC domain, reset after power up

2nd source: 82.20013.121

Power Good 3V

0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms

2013/06/26 Change time sequence for PCH_PWRGD Ryan

20131023 Madrid_SA Charles
check list modify ;
cancel 1.05VTT_PWRGD

PWRBT Signal

To SIO

To PCH

EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable

EC Board ID Description

	ID2 bit1	ID1 bit0
SA	0	0
SB	0	1
-1A	1	0
-1	1	1
-2	0	0

	ID3
W/ Scalar	1
W/O Scalar	0

(GP33) bit1(GP34) bit0(GP35)

ID3 ID2 ID1

Reserved MOS for debug, follow Petra2381
Damon SB Modify 01/25

20121011_aPisa_SB Charles Add Board 3

20121023_aPisa_SB Charles define ID3

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ECIO (KBC KB9028)

Size: C | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2013 | Sheet 24 of 55

SPI_CS_CPU_N0_R
SPI_SO_ROM
SPI_WP_ROM
SPI_HOLD_ROM
SPI_CLK_ROM
SPI_SI_ROM

RTC_DET#

Main Func = SPI Flash

SPI FLASH ROM (16M byte) for PCH

SPI ROM Equal length need to less than 500mil

18
18
18
18
18
20,25

3D3V_S5
3D3V_S5
3D3V_S5
3D3V_S5

Main Func = RTC

RTC BATTERY

3D3V_AUX_S5

Follow Mocha,
Damon SB Modify 01/12

Davy 0515

3D3V_RTC_VCC

3D3V_RTC_AUX

Width=20mils

20,25

RTC_DET#

3V / 4mA

Change BTT1 CONN to (062.70001.0081), follow CE advice
Damon Wei SA Modify 2018/12/07

Clear CMOS

18 RTC_RST#

RTC Reset follow Eiffel215i_Kblu
Damon Wei SA Modify 2018/10/18

1-2 short :Clear CMOS
1-2 open : Normal (Default)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

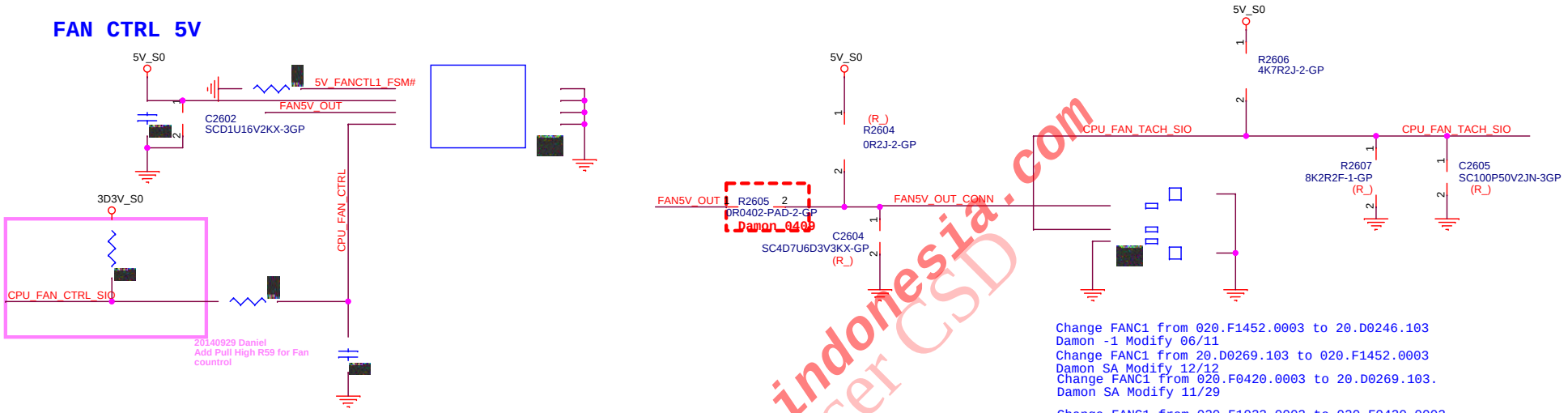
Title: ***Flash/RTC***		
Size: A3	Document Number: **Eiffel-2**	Rev: **-1**
Date: Thursday, June 27, 2019	Sheet 25 of 106	

SSID = Thermal

Fan Controller

CPU_FAN_CTRL_SIO 24
CPU_FAN_TACH_SIO 24

FAN CTRL 5V



Change FANC1 from 020.F1452.0003 to 20.D0246.103
Damon -1 Modify 06/11
Change FANC1 from 20.D0269.103 to 020.F1452.0003
Damon SA Modify 12/12
Change FANC1 from 020.F0420.0003 to 20.D0269.103.
Damon SA Modify 11/29

Change FANC1 from 020.F1033.0003 to 020.F0420.0003.
Damon SA Modify 11/17

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Flash/RTC***	
Size B	Document Number **Eiffel-2**	Rev **-1**
Date: Thursday, June 27, 2019	Sheet 26 of 106	

SSID = AUDIO

Damon SB Modify 01/21

5V_S5

5V_S0 Follow Vendor Advice Damon SA Modify 11/22

Damon 0409

Note:
5V_AUDIO_S0 must be with 1.05A current budget for PVDD.

5V_AUDIO_S0

Digital Moat

Analog Moat

3D3V_S0

3D3V_AUDIO_S0

3D3V_S5

Damon -1 Modify 06/17

Close to Pin46

Change to Show Pad,
Damon 1A Modify 04/09

AUD_AGND

MOAT

MOAT

Follow Eiffel215i KBLU
Damon SA Modify 11/13

Follow Eiffel215i KBLU
Damon SA Modify 11/13

Fix Vout=1D5V
Imax=300mA
OCP = 400mA

Close to Pin41

Close pin36

1D8V_S0

1D8V_AUDIO_S0

1D8V_S5

Close pin40

Damon -1 Modify 06/17

Layout Note:
Place close to Pin 26

5V_AUDIO_S0

Analog Moat

1D8V_AUDIO_S0

5V_AUDIO_S0

Digital Moat

Damon 0409

Follow Vendor advice
Damon SA Modify 11/23

5V_AUX_S5

3D3V_AUDIO_S0

3D3V_AUX_S5

Damon 0409

1D8V_AUDIO_S0

3D3V_AUDIO_S0

Damon 0409

Follow vendor advise for co-lay
Damon SA Modify 11/21

NOTE:
ALC255-CG-GP-U
P/N:071.00255.0003
ALC256M-CG-GP
P/N:071.00256.0003

Close to Pin1

Damon 0409

Damon 0409

Co-lay ALC255 and ALC256M
Damon SA Modify 11/13

placed nearby codec PIN12

HDA_BITCLK_CODEC 19
HDA_SYNC_CODEC 19
HDA_SDIN0_CPU 19
HDA_SDOUT_CODEC 19

SIO_AUDIO_MUTE 24

DMIC_CLK_CON 30
DMIC1_DATA_CON 30
AUD_HP1_JACK_L2 29
AUD_HP1_JACK_R2 29
AUD_HP1_JD# 29
RING2 29
SELEEVE 29

HDA_SPKR 15,19
AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_R+
AUD_SPK_R-

HDA_RST_N_CODEC 19

PM_SLP_S3# 17,24,40,52,68

AUD_AGND 29

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Codec_ALC256)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 27 of 106

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio (RSVD)*

Size	Document Number	Rev
B	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 28 of 106

SSID = AUDIO

Speaker

AUD_SPK_L-
AUD_SPK_L+
AUD_SPK_R-
AUD_SPK_R+

2019/01/14 Damon SB Modify
L2904/L2905/L2906/L2907 change from 68.00335.151 to 68.00335.091 by F7

L2904 BLM18BD601SN1D-GP
(68.00335.091)

L2905 BLM18BD601SN1D-GP
(68.00335.091)

EC2904
SC1KP50V2KX-1GP
(78.10224.2FL)

2017/02/28 1A
SPK1 F7 change from 20.F1819.004 to (020.F0420.0004)

Change SPK1 CONN to 020.F0420.0004, follow Eiffel215_kblu.
Damon Wei SA Modify 2018/10/18

Change SPK1 CONN to 020.F1076.0004, follow CE advice
Damon Wei SA Modify 2018/12/07

RING2
AUD_HP1_JACK_L2
AUD_HP1_JD#
AUD_HP1_JACK_R2
SELEEVE

AUD_AGND

R2905
75R2J-1-GP

Follow Eiffel215 KBLU
Damon SA Modify 11/15

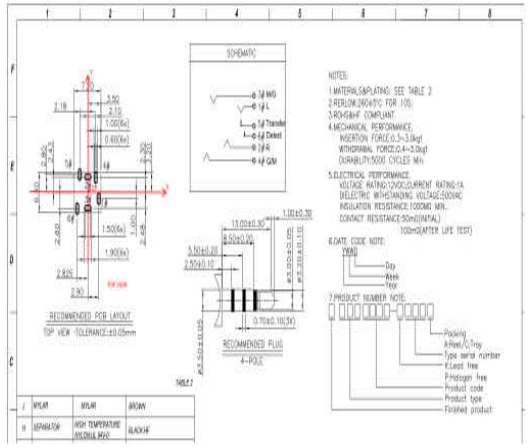
EC2910
SC1KP50V2KX-1-GP
(78.10224.2FL)

AUD_AGND

HP-Out-Right
HP-Out-Left
Ring2
Sleeve

Change AUDS1 CONN to (022.10002.0C41), follow CE advice
Damon Wei SA Modify 2018/12/07

Change AUDS1 CONN to 022.10002.0K41, follow Eiffel215a.
Damon Wei SA Modify 2018/10/18



R2921
0R0402-PAD-2-GP

Damon 0410

AUD_AGND

Damon 0410

AUD_AGND

Damon 0410

AUD_AGND

Follow Eiffel215 KBLU
Damon SA Modify 11/15

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio (Speaker/HPMIC)**

Size: C | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 29 of 106

USB2.0 Port7 -> CAM

DMIC

DMIC1_DATA_CPU 19
DMIC1_CLK_CPU 19
DMIC1_DATA_CON 27
DMIC_CLK_CON 27

16 CCD_USB20_N
16 CCD_USB20_P

Damon 0409

Close CAM1 CONN

Add C3008 C3009 PD for EMC advice,
Damon 1A Modify 03/29

Close CAM1 CONN

change to Co-lay
Damon SA Modify 11/26

Damon 0409

3D3V_S5

USB redriver for CAM

Damon 01/16

EL3001
COIL-90OHM-100MHZ-5-GP

3D3V_CAM

Add redriver for CAM,follow Cartier.
Damon SA Modify 11/20

CAM1 CONN

PWR_DMIC
3D3V_CAM

01/15 Damon SB Modify
Change Connector to P/N:020.F1064.0008

3D3V_S0
3D3V_S5

Damon 0409

12/3 changes to 69.48001.081

3D3V_CAM

C3004 SC22UD3EX3WX-1GP
C3005 SCD1U16V2KX-3GP

3D3V_S5

PWR_3D7V_DMIC
3D3V_S0

PWR_DMIC

Damon SA Modify 11/14

Change Power source from 5V to 3.3V and add F8
20131023 Kenyon
12/25 changes to 69.48001.081 symbol

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (RSVD)
Size: C
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Rev: -1
Date: Thursday, June 27, 2019
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Giga LAN

PCI-E
LAN_PCIE_RX_N_C
LAN_PCIE_RX_P_C
LAN_PCIE_TX_N_C
LAN_PCIE_TX_P_C

CLOCK
LAN_CLK_CPU_N_C
LAN_CLK_CPU_P_C
LAN_CLKREQ_CPU_N_C

LAN
PLTRST_LAN_N
PCIE_WAKE#
LAN_WAKE#
PLT_RST#

Bogis 20121222
Change solution
to RTL8111GA

Colse to the AVDD33
pin location

11/21 reserved for vendor request
C302 close to Pin11 (AVDD33)

Colse to the AVDD10
pin location

Colse to
the
pin22

Reserve for
RTL8111G/GS/GA

Reserve for
RTL8111GA

LAN_CLKREQ_CPU_N

Damon 0909

Add TP26 in layout

Mount for RTL8111G /RTL8111H

Mount for RTL8111GS/RTL8111GA ONLY

2018/01/03 Damon 1A Modify
Follow E1771A1151_REV

Close
to LAN
chipset

IC	P/N	L21	R269	C270
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R
RTL8111H	071.8111H.0003	R	M	R

M:Mount
R:Reserved

Change to 68.IM601.301 Vendor advise
Damon Wei SB Modify 20190114

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

EC3107
R3158
Unmount EC3101 ~ EC3108, follow Vendor Request.
Damon Wei SA Modify 2017/11/10

XTAL
12.18 Javon modify follow Copper
SB_1116
SC_1207
SB_1121
C3116 C3117change from 22pf to 18pf,
R3156 change to 1.0K,follow vendor suggestion
Damon Wei -1 modify 2016/03/12

X3101
082.30005.0B21 HOSONIC
082.30005.0911 MURATA
082.30005.0A81 HARMONY

12/4 Derek remove R273 short pad
2015/05/05 Jorly
Unmount for LOW MODE

2017/09/15 Only Mount C3118,C3119
Damon Wei SA Modify

11/18 Akuan dummy

Davy 0712
Leakage from LAN_WAKE# to 3D3V_LAN
1K 0.4V --> 10K 0.054V

Layout close
to
CPU/FCH/PCH

open-drain

Damon 0618

Lan_WAKE follow Steffi
2017/10/12 Damon SA Modify

Damon 0617

Connect to SIO GPIO
S3/S4/S5 = Low
Others = High
To meet Tpvperl spec > 100ms
(Power Stable to PERST Inactive)

Damon 0410

Check with Kelia the LAN reset issue

2014/09/01 Daniel
Follow Lijiang LAN Surge Solution Cost Down

Lan Surge

Reserve EMI
CMN Choke

Change to suitable type
2013/05/3 Kenyon

LAN Power

Modify LAN PWR delay circuit,for Rising time >1ms
Damon Wei 1A 19/04/08

+3VM_LAN rise time:
0.5mS ~ 100mS

S0:3D3V_S5
S3:3D3V_S5
S4:3D3V_S5
S5:3D3V_S5
EUP:0

C3155
SC1U10V2KX-1GP

2010/09/20
LAN surage solution

2011/06/26

PCB

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

75.01215.07C

75.01215.07C

2017/04/29
GD3203/GD3204/GD3205/ change to (75.00009.070),F7 for common part

RJ1

2016/12/27
RJ1 symbol change to 062.10005.0371

2017/02/17
RJ1 dot F7 062.10032.0041

2016/11/16
Vendor advised

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 31 of 46

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*LAN (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
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Card Reader

USB 2.0

CR_USB20_P 16
CR_USB20_N 16

EMI/ESD near Chip

EC3321 1 2 SC5P50V2CN-2GP (R_)
EC3321 1 2 SC5P50V2CN-2GP (R_)

2IN1 (SD/MMC) Combo Net

3D3V_MAIN_MSSD 3D3V_CARD

C3301 SC1U10V2KX-1GP
6K2R2F-GP 1 2 R3301
Near the chip

RTD5176 Power

3D3V_S0
3D3V_MAIN_MSSD

EMI reserve

R3304 1 2 0R0402-PAD-2-GP
R3305 1 2 0R0402-PAD-2-GP
Damon 0410

3D3V_MAIN_MSSD Near the pin5
3D3V_MAIN_MSSD Near the pin6
3D3V_MAIN_MSSD Near the pin8
C3306 SC1U10V2KX-4GP

2IN1 CONN (SD/MMC)

3D3V_CARD
R3302 2 1 0R0603-PAD-2-GP-U
C3314 SCD1U16V2KX-3GP
R3311 (R_) 100KR2F-L1-GP
C3312 (R_) SCD1U16V2KX-3GP

Select normal close
SD_CD/WP internal pull high
insert SD card => SD_CD low

Change from 62.10051.H51 to 062.10002.0561 ,follow CE suggestion
Damon SA Modify 12/12
Change to 62.10051.H51,follow eiffel215i-kblu
Damon SA Modify 10/26

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER (RSVD)
Size: C
Document Number: Eiffel-2
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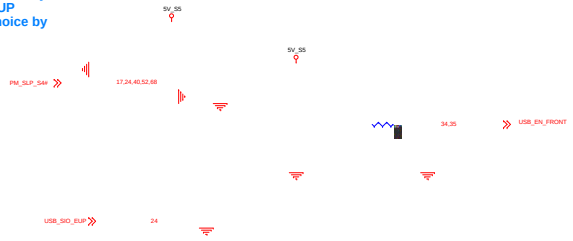
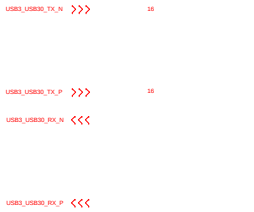
USB Power Enable

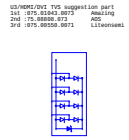
	S5	S4	S3-S0		S5	S4	S3-S0	Status
SLP_S5_N	L	L	H	USB_EN_R	L	L	H	No Support S4/S5 USB wake up
USB_SIO_EUP	L/H	L/H	L	USB_EN_R	L	H	H	Support S4/S5 USB wake up

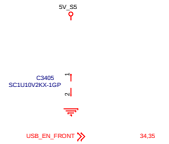
S4, S5 --> choice by USB_SIO_EUP
S3-S0 --> choice by SLP_S5_N



USB3.0 Port

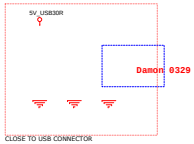


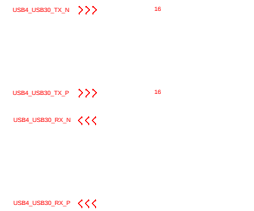


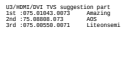


change U3401 from 074.00524.0B9F to common part
074.51712.009F (2nd source:074.09742.0A9F)
Damon Wei SA Modify 2017/11/16

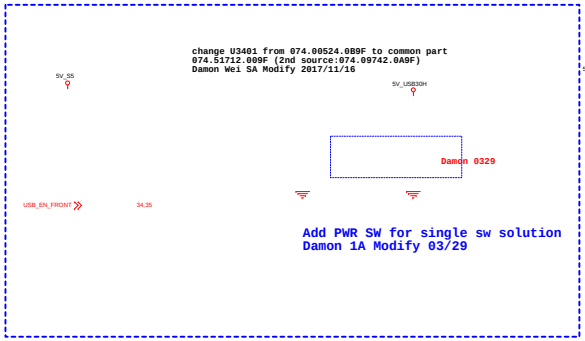
USB3R3 change to USB3.0 P/N:022.10005.0ZQ1
Damon Wei SA Modify 2019/01/08





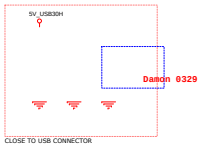


change U3401 from 074.00524.0B9F to common part
074.51712.009F (2nd source:074.09742.0A9F)
Damon Wei SA Modify 2017/11/16



Add PWR SW for single sw solution
Damon 1A Modify 03/29

USB3R4 change to USB3.0 P/N:022.10005.0ZQ1
Damon Wei SA Modify 2019/01/08



<Variant Name>

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD)

Size	Document Number	Rev
D	Eiffel-2	-1

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USB3.0 Side Port

USB1_USB30_TX_N 16
USB1_USB30_TX_P 16
USB1_USB30_RX_N 16
USB1_USB30_RX_P 16
C3514 SCD1U16V2KX-3GP
USB1_USB20_P 16
USB1_USB20_N 16

U3/HDMI/DVI TVS suggestion part
1st :075.01043.0073 Amazing
2nd :75.00888.073 ADG
3rd :075.00550.0071 Liteonsemi

5V_S5
USB_EN_FRONT 34,35

change U3503 from 074.00524.0B9F to common part
074.51712.009F (2nd source:074.09742.0A9F)
Damon Wei SA Modify 2017/11/16

5V_USB30F
Damon 0329
CLOSE TO USB CONNECTOR

Change USB3R1 CONN to 022.10005.0F41, follow CE advice
Damon Wei SA Modify 2018/12/21

5V_USB30F

U2/LAN/DMIC TVS suggestion part
1st :075.00904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

Change to 220nf,follow PDG.
Damon Wei SA Modify 2018/10/18
Change to 100nf,for GEN1
Damon Wei SA Modify 2018/12/04

USB2_USB30_TX_N 16
USB2_USB30_TX_P 16
USB2_USB30_RX_N 16
USB2_USB30_RX_P 16
USB2_USB20_P 16
USB2_USB20_N 16

U3/HDMI/DVI TVS suggestion part
1st :075.01043.0073 Amazing
2nd :75.00888.073 ADG
3rd :075.00550.0071 Liteonsemi

5V_S5
USB_EN_FRONT 34,35

change U3503 from 074.00524.0B9F to common part
074.51712.009F (2nd source:074.09742.0A9F)
Damon Wei SA Modify 2017/11/16

5V_USB30E
C3520 SCD1U16V2KX-3GP
Damon 0329
CLOSE TO USB CONNECTOR

Add PWR SW for single sw solution
Damon 1A Modify 03/29

5V_USB30E

U2/LAN/DMIC TVS suggestion part
1st :075.00904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

Change USB3R2 CONN to 022.10005.0F41, follow CE advice
Damon Wei SA Modify 2018/12/21

5V_USB30E
Damon 0329

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB (USB3.0)		
Size: D	Document Number: Eiffel-2	Rev: -1
Date: Thursday, June 27, 2019	Sheet 35 of 100	

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (USB Charger)***

Size	Document Number	Rev
B	**Eiffel-2**	**-1**

Date: Thursday, June 27, 2019 Sheet 36 of 106

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 37 of 106	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB (RSVD)	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 38 of 106	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Sequence (RSVD)***	
Size: A4	Document Number: **Eiffel-2**	Rev: **-1**
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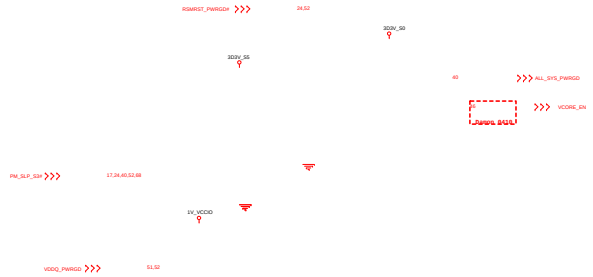
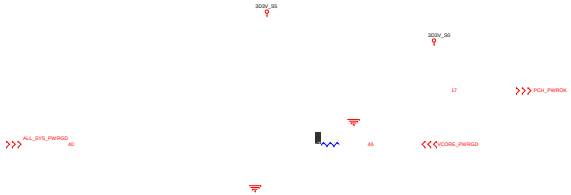
Power Sequence

VCORE_EN



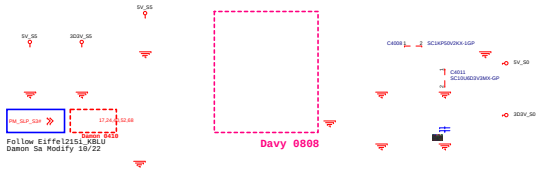
VCORE_PWRGD



VCCST_PWRGD

VCCST_PWRGD circuit follow Strongbow
Damon SA Modify 11/02

3D3V_S0 & 5V_S0



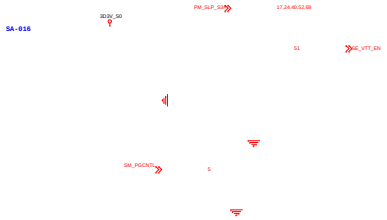
Follow Eiffel21S1_KBLU
Damon Sa Modify 10/22

DDR4 Power Sequence

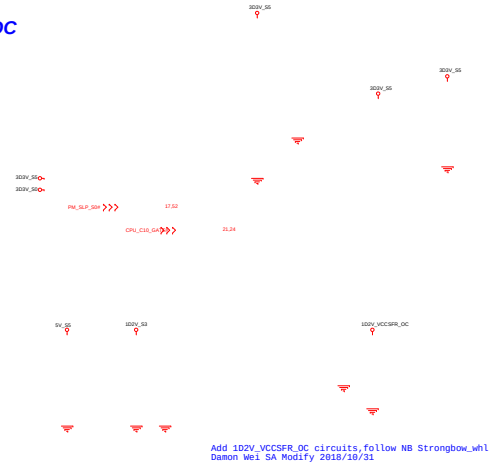
VPP(2.5V) enable

VDDQ(1.2V) enable

VTT(0.6V) enable



VccPLL_OC



Add 1D2V_VCCSFR_OC circuits,follow NB Strongbow_whl
Damon Wei SA Modify 2018/10/31

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Sequence (RSVD)***	
Size: A4	Document Number: **Eiffel-2**	Rev: **-1**
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*INT IO (RSVD)*	
Size: A4	Document Number: Eiffel-2	Rev: -1
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DC Jack

19V_AD_JK

Soft start

19V_AD_JK_R

19V_ADP

19V_ADP

19V_DCBATOUT

2017/10/23 Damon Wei SA Modify

Change PU4301 to 084.04305.0037
Damon SB Modify 01/18

2013/04/18 David
Follow Pisa PR9 mount 10k ohm
to fix AC off issue
2013/12/11 Derek
un-mount PR14 for S5 current over SPEC 7mA

OCP

19V_AD_JK

SIZE 2512
0.01OHM 2W

19V_AD_JK_R

GAIN1= VO/(V2-V1)=R2/R1

Del NONOCP Co-lay 0Ohm
Damon SA Modify 11/17

R2

Damon 0410

19V_AD_JK_R

GAIN2= 1+R2/R1

V1

V2

R1

VO

20140303 Madrid -1
Charles
modify to 30Kohm

R2

R1

R2

20140303 Madrid -1
Charles
modify to 300Kohm

19V_AD_JK_R

19V_AD_JK_R

19V_AD_JK_R

19V_AD_JK_R

RH

20131127 Madrid SB Charles
follow seattl OPC control

(O_63.R0034.1DL)
PR4313
8K2R2F-1-GP

5V_S5

3D3V_S5

RL

09.1071D.B0L
Alt:

	RH	Vc	10%
135W:	6.04k	5V	~121W
90W:	6.04k	3.3V	~81W
65W:	0	3.3V	~60W

19V_AD_JK_R

20131112 aPisa -1A Charles
Add a pull low resistor for
65W

3,24

PROCHOT_N_OCP

PWROK3_1_R

24

SYS_PWROK

17,24,68,99

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (DC IN/BAT CON)

Size: C | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 43 of 106

PWR_3D7V_ PWR_CAM

Follow Cartier238i WHL
Damon SA Modify 11/26

Iomax=1A

5V_S5

PWR_3D7V_VIN

2.2uH,
DCR=18~20mohm,
Idc=8A, Isat=14A
6.86*6.47*3

PWR_3D7V

PWR_3D7V_DMIC

3D3V_S5

PR4402
10KR2J-3-GP
(R_)

R1

0.6* 1+R1/R2)
=3.741V

R2

5V_S5

change to R4402 10K,PC4402 0.1uF for sequence,
Damon SA Modify 11/20

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power (CHARGER BQ24780)	
Size: Custom	Document Number: Eiffel-2	Rev: -1
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3D3V_S5 PWR_3D3V 3D3V_S5 PWR_3D3V 19V_DCBATOUT PWR_DCBATOUT_3D3V

5V/3V ENABLE CONTROL

EC_EUP_EN 24,52

5V/3V POWER GOOD

3V_5V_PWRGD

19V_DCBATOUT PWR_DCBATOUT_5V PWR_5V 5V_S5 PWR_5V 5V_S5

PWR_DCBATOUT_3D3V

Iccmax=7.3A
OCP>10.95A

PWR_3D3V

PT4501
ST150U6D3VDK-GP

2017/02/16
Change PT4501 to POSCAP 077.51571.0001
2018/12/04
Change PT4501 to 79.15710.2BL

Cyntec. 7 X 7X 3.0 mm
DCR: 18～20 mohm
Idc : 8A , Isat : 14A

PL4501

IND-2D2UH-46-GP-U1

PC4512
SCD1U25V2KX-GP

19V_DCBATOUT

PC4505
SCD1U25V2KX-GP

PR4504
84K5R2F-GP

3D3V_AUX_S5

5V_AUX_S5

PWR_DCBATOUT_5V

PC4510
SC10U25V5KX-GP

Cyntec. 7 X 7X 3.0 mm
DCR: 18～20 mohm
Idc : 8A , Isat : 14A

Iccmax=6.25A
OCP>9.375A

PWR_5V

Change to 35.4K
Damon -1 Modify 06/20

Vout=2*(1+R1/R2)
=5.08V

PR4507
10KR2F-2-GP

3D3V_AUX_S5 3D3V_S5

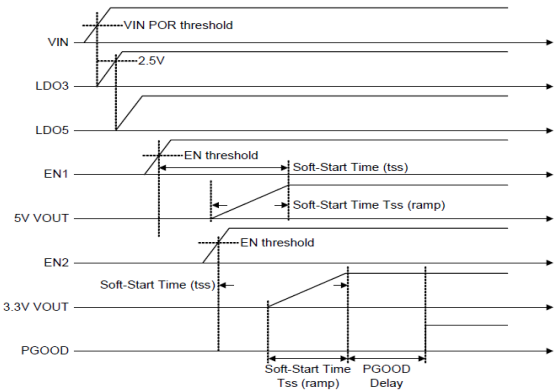

Figure 6. RT6575B Timing

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6575D_5V/3D3V_SB

Size: Custom | Document Number: Eiffel-2 | Rev: -1

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OFFPAGE

SVID_ALERT#_CPU 7
SVID_CLK_CPU 7
SVID_DATA_CPU 7
VCORE_PWRGD 40
VCORE_EN 40
PROCHOT#_CPU_R 8
PWR_VCC_SENSE 7
PWR_VSS_SENSE 7
PWR_VSSGT_SENSE 8
PWR_VCCGT_SENSE 8
PWR_VSSSA_SENSE 8
PWR_VCCSA_SENSE 8

Main Func = CPU_CORE

confirm with FE
3D3V_S0

confirm with FE
1V_VCCSTG

confirm with FE
1V_VCCST

confirm with FE
19V_DCBATOUT
5V_S5

PR4608 93K1R2F-L-GP
PC4604 SC330P50V2KX-3GP
Place near high side MOSFET of Phase1(PU4702)

PR4611 NTC-10K-29-GP-U
B=3370K
Place near Phase1 choke(PL5001)
PWR_VCCSA_ISUMN
PWR_VCCSA_ISUMP

20170109 Power demand 330K -> 330 ohm
PR4620 330R2F-GP

David 02/15

PC4616 SC1KP50V2KX-L-1-GP
DY
(R_)

20190215 1A LL change 1.54K to 2.15K
20190215 1A LL change 1.32K to 1.45K

PWR_VCCSA_PWM
PWR_VCCSA_FCCM

1V_CPU_CORE

PC4622 SCD01U25V2KX-3GP
PWR_VCCGT_ISUMP

PR4646 NTC-10K-29-GP-U
B=3370K
Place near Phase1 choke(PL4702)
PWR_VCCGT_ISUMN

20170109 Power demand 360K -> 360 ohm
20170111 Power demand 255K -> 267 ohm
20190215 267 ohm -> 374 ohm (IA IMON)

PWR_VCCGT_FCCM#
PWR_VCCGT_PWMA
PWR_VCCGT_PWMB

PWR_VCCGT_ISEN1
PWR_VCCGT_ISEN2

Place near high side MOSFET of Phase1(PU4801)

20170111 Power demand 2K -> 1.65K ohm
20190215 47 LL change 1.65K to 1.78K

1V_VCCGT

074.95859.0D33

PWR_VCORE_PWM
PWR_VCORE_FCCM#

Base on PROG1 & 2
PWR_VCORE_ISUMN
PWR_VCORE_ISUMP

PR4650 NTC-10K-29-GP-U
B=3370K
Place near Phase1 choke(PL4801)

	U22	U42
PC4625	DY	0.022u(78.22321.2FL)
PC4626	DY	0.022u(78.22321.2FL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL)	316(64.31605.6DL)
PC4630	0.1u(78.10422.5FL)	0.1u(78.10422.5FL)
PC4628	0.01u(78.10324.L0L)	0.022u(78.22321.2FL)
PC4653	DY	47n(78.47322.2FL)
PR4633	1.54K(64.15415.6DL)	3.01K(64.30115.6DL)
PR4608	88.7K(64.88725.6DL)	88.7K(64.88725.6DL)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: (ISL95829_CPUCORE1/3)
Size: Custom | Document Number: Eiffel-2 | Rev: -1
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Main Func = CPU_CORE

075.00998.0073
SiZ998DT
Vgs @ 4.5V
HS:
Id =20A
Rds(on) = 6.5~10mohm
LS:
Id = 60A
Rds(on) = 3~3.8mohm

PWR_DCBATOUT_VCOREA

19V_DCBATOUT

PWR_DCBATOUT_VCOREA

5V_S5

PR4702
0R0402-PAD-1-GP

PWR_VCCGT_PWMA

PWR_VCCGT_FCCM#

46,47

Cyntec 6.8mm x6.4mmx4.0mm
DCR: 0.66m Ohm +/-7%
Idc : 26A , Isat : 52A

1V_CPU_CORE

SKL U42
Icc(max)=70A
TDC=48A

Confirm with EE
22uF/0805
total 32pcs
(78.22610.L2L)

PWR_VCCGT_ISEN1
PWR_VCCGT_ISUMP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN2

46,47

PWR_DCBATOUT_VCOREB

19V_DCBATOUT

PWR_DCBATOUT_VCOREB

PR4713
0R0402-PAD-1-GP

PWR_VCCGT_PWMB

PWR_VCCGT_FCCM#

5V_S5

PC4708
SC1U10V3KX-1-GP

Cyntec 6.8mm x6.4mmx4.0mm
DCR: 0.66m Ohm +/-7%
Idc : 26A , Isat : 52A

1V_CPU_CORE

PANASONIC
ESR: 9
mohm

PWR_VCCGT_ISEN2
PWR_VCCGT_ISUMP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN1

46,47

<Variant Name>

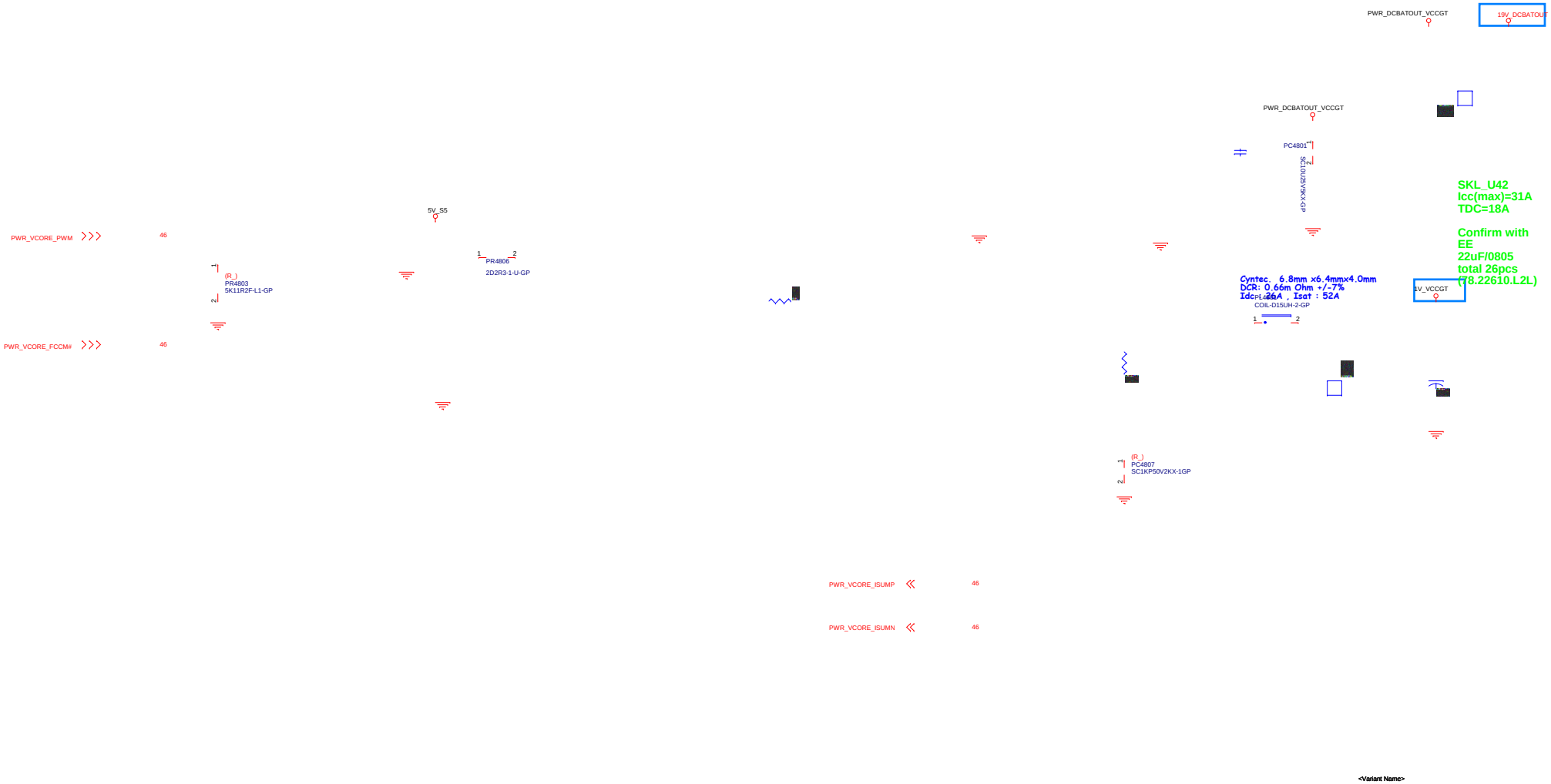
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (ISL6208B_CPUCORE2/3)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2013 | Sheet 47 of 56

Main Func = CPU_CORE



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	POWER (AOZ5049Q_VCCGT(3/3))	
Size: Custom	Document Number: Eiffel-2	Rev: -1
Date: Thursday, June 27, 2019	Sheet 48 of 106	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power (EE Reserved)**

Size	Document Number	Rev
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Date: Thursday, June 27, 2019 Sheet 49 of 106

Main Func = CPU_CORE

19V_DCBATOUT

PWR_DCBATOUT_VCCSA

PWR_DCBATOUT_VCCSA

SKL_U42_35W
Icc(max)=5.1A
TDC=3.7A

Confirm with EE
22uF/0805 total 5pcs
(78.22610.L2L)

5V_S5

PC5001
SC2D2U10V3KX-1GP

PR5001
2D2R3-1-U-GP

PC5005
SCD22U25V3KX-GP

PC5002
SC10U25V5KX-GP

(R_)
PC5003
SC10U25V5KX-GP

(R_)
PC5004
SCD1U25V2KX-GP

Cyntec.
6.6mmx7.3mm x3.0mm
DCR: 4~4.2 mohm
Idc : ~~17.5A~~ , Isat : 20A.

PR5001

IND-D47UH-22-GP-U

1V_VCCSA

PWR_VCCSA_PWM

PWR_VCCSA_FCCM

46

46

If need support PS4 mode
please change to ISL95808

46 PWR_VCCSA_ISUMP

46 PWR_VCCSA_ISUMN

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (ISL6208B_VCCSA)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

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SSID = PWR.Plane.Regulator_1p2v0p6v

VDDQ POWER GOOD
VDDQ_PWRGD 40,52

VDDQ ENABLE CONTROL
VDDQ_EN 40,51,54

VID
Logic-High = 0.75V
Logic-Low = 0.3V
5V_S5

OCP setting

3D3V_S5

5V_S5

PC5108
SC1U10V2KX-1GP
SC-027
SC-038

2017/04/19
PR5127 change to short pad

Freq. setting
750K -> 350K Hz
PWR_DCBATOUT_VDDQ

PR5115
2D2R5J-1-GP

19V_DCBATOUT
PWR_DCBATOUT_VDDQ

84.04C10.037 NTMFS4C10N
Rds(on) = 5.8~6.95 mohm,
Vgs=10V, I-D = 30A,
Qg = 18.9nC
Vgs=10V, Vds=15V, I-D=30A

84.04C06.037 NTMFS4C06N
Rds(on) = 3.2~4.0 mohm,
Vgs=10V, I-D = 30A,
Qg = 29nC
Vgs=10V, Vds=15V, I-D=30A

PWR_DCBATOUT_VDDQ

VIN RIPPLE CURRENT Imax=2.32A

2016/12/28
DEL PR5112

2016/12/28
DEL PR5107

1.0uH,
DCR=9~10mohm,
Idc=11A, Isat=22A

Idesign=9.5A
14.25A<OCP<19A
V_SM

V_SM

Need EE confirm

VDDQ_EN 40,51,54
Damon 0409
SC-027
SC-037
2017/04/19
PR5113/PR5114 change to short pad
S5

SE_VTT_EN 40
PR5114
0R0402-PAD-2-GP
Damon 0409
S3

PWR_VDDQ_VTT

Close to output cap pin1, not inside of the output cap
V_SM

R1

R2

Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 15.8K / 20K)
= 1.2V

VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on

SB-021

330uF/2V/7.3*4.3*1.9
ESR=9mohm
Iripple=3A

V_SM
1D2V_S3

SB-021
SB-033
1A-016

Vout = 0.6V
Iomax = 0.75A
0D6V_VREF_S0

PWR_VDDQ_VTT

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title
POWER_MEM&VTT_RT8231A_1D2V

Size A2 | Document Number Eiffel-2 | Rev -1

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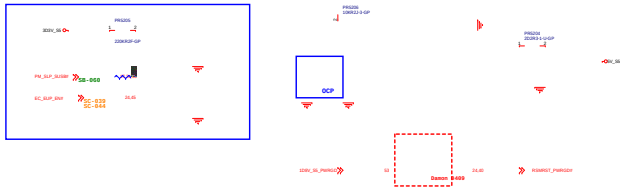
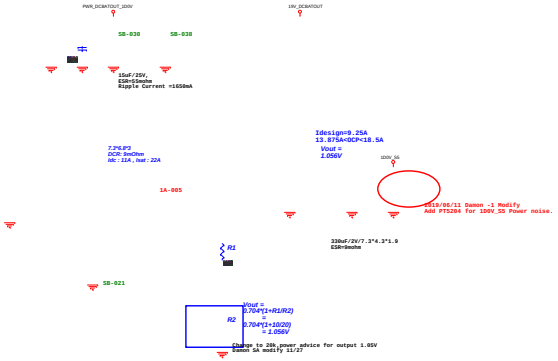
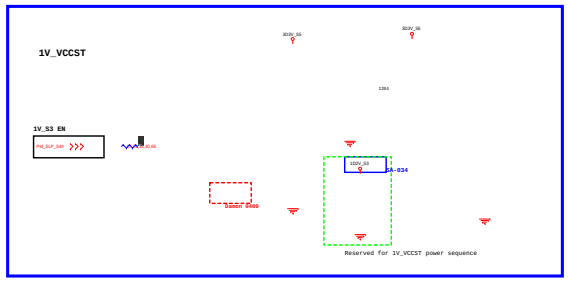
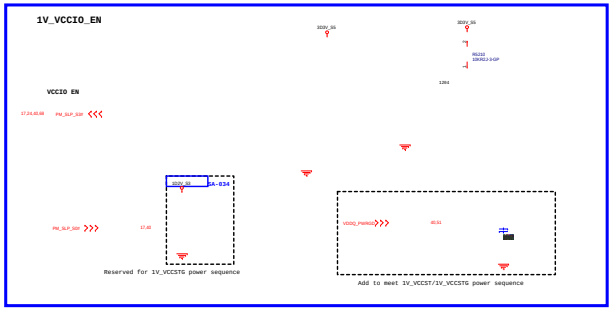
SSID = PWR.Plane.Regulator_1p0v

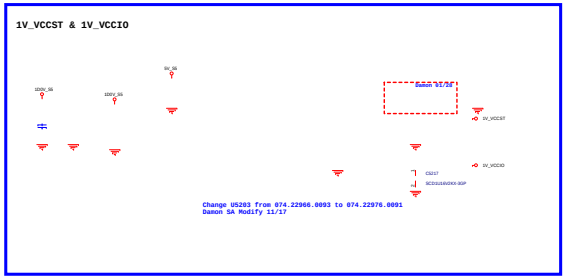
RT8237 for 1D0V











<Variant Name>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D0V_S5/1V_VCCST/1V_VCCIO

Size: A3 | Document Number: Eiffel-2 | Rev: -1

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PWR_1D8V

2016/12/19 change from 3D3V_A to 3D3V_S5

PWR_1D8V_VIN

3D3V_S5

5V_S5

3D3V_S5

Iomax=0.64A

PWR_1D8V

1D8V_S5

1D8V_S5_PWRGD

52

3V_5V_PWRGD

Change to 3V_5V_PWRGD
Damon SA Modify 11/17

Add 1k Res for RC delay
Damon SA Modify 11/17

PM_SLP_SUSB#

17,24,52

R1

PR5304
12K7R2F-GP

R2

Vo=0.8*(1+(R1/R2))=1.81 V

1D8V_S5 to 1D8V_S0

3D3V_S5

5V_S0

1D8V_S5

Damon 01/16

R5301 10KR2J-3-GP

3D3V_S0

(R_)
PC5307
SCD1U25V2KX-GP

Damon 01/16

1D8V_S0 for ALC55 AVDD2

1D8V_S0

Follow Cartier238
Damon SA Modify 11/13

Add 10K PD for 1D8V_S0 discharge
Damon SB Modify 01/16

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D8V_S5(APL5930)	
Size A3	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 53 of 106	

PWR_2D5V_VPP

2D5V POWER Enable

2D5V_S5_EN 40

2D5V POWER GOOD

2D5V_S5_PWRGD 40

40,51 VDDQ_EN

S5

5V_S5

3D3V_S5

PRS402
100KR2F-L1-GP

PRS405
100KR2J-1-GP

PC5406
SCD1U25V2KX-GP

2017/02/24
PR5403 changed from 21k to21.5k

PWR_2D5V_VIN

PC5401
SC22U6D3V3MX-1-GP

2016/12/19 change from 3D3V_A to 3D3V_S5

3D3V_S5

Iomax=2.24A

PWR_2D5V_VPP

2D5V_S3

R1

(R_)
PC5405
SC100P50V2JN-3GP

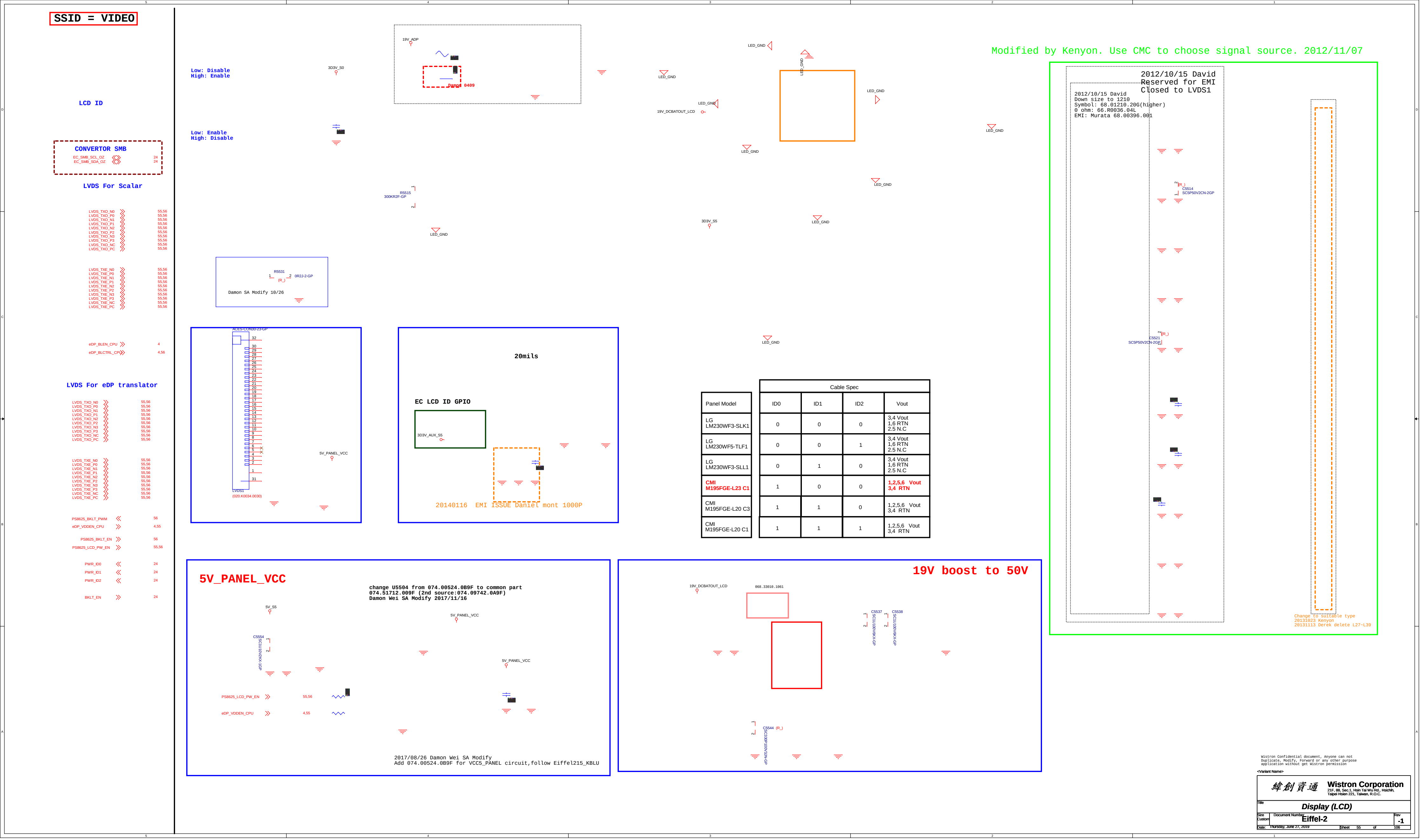
R2

Vo=0.8*(1+(R1/R2))=2.52 V

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power (RSVD)	
Size C	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 54 of 106	



Panel Model	ID0	ID1	ID2	Vout
	Cable Spec			
LG LM230WF3-SLK1	0	0	0	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF5-TLF1	0	0	1	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF3-SLL1	0	1	0	3,4 Vout 1,6 RTN 2,5 N.C
CMI M195FGE-L23 C1	1	0	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C3	1	1	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C1	1	1	1	1,2,5,6 Vout 3,4 RTN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

2012/10/14 David
Follow design guide

eDP_AUX_CPU_N
eDP_AUX_CPU_P
C5601 2 SCD1U16V2KX-3GP eDP_AUX_CON_N
C5602 2 SCD1U16V2KX-3GP eDP_AUX_CON_P

eDP_TX_CPU_N0
eDP_TX_CPU_P0
C5603 2 SCD1U16V2KX-3GP eDP_TX_C_N0
C5604 2 SCD1U16V2KX-3GP eDP_TX_C_P0

eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_TX_C_N1
eDP_TX_C_P1

4,56 eDP_HPD_CPU
PS8625_BKLT_PWM 55
PS8625_LCD_PW_EN 55
PS8625_BKLT_EN 55
eDP_BLCTRL_CPU 4,55
R5601 2 0R0402-PAD-2-GP DP_VARY_BL_R

Damon 0310

LVDS_TXO_N0 ... LVDS_TXO_PC 55
LVDS_TXE_N0 ... LVDS_TXE_PC 55
3D3V_S5

Damon 0310

3D3V_2136
AVCC
3D3V_EDP_VDDIO
C5609 SCD1U16V2KX-3GP
C5610 SCD1U16V2KX-3GP
Closed to RTD2136 pin 5

L5602 HCB1608KF121T30-GP
DVCC
3D3V_EDP_VDDIOX
C5615 SCD1U16V2KX-3GP
C5616 SC22U6D3V3MX-1-GP
2015/06/23 C518 change to 78.22610.5BL
Closed to RTD2136 pin 22
Closed to RTD2136 pin 18

2015/05/23
C524/C526 Change to 78.10623.51L

1D2V_EDP
C5617 SC10U25V6KX-GP
C5618 SCD1U16V2KX-3GP
C5619 SCD1U16V2KX-3GP
C5620 SCD1U16V2KX-3GP
Closed to RTD2136 pin 15
Closed to RTD2136 pin 11
Closed to RTD2136 pin 43

TSMT_SMB_SDA_U_R R5610 1 2 4K7R2J-2-GP
MODE_CFG0 R5611 1 2 4K7R2J-2-GP
3D3V_EDP_VDDIO

MODE_CFG1(PIN48)	MODE_CFG0(PIN47) 0	MODE_CFG0(PIN47) 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

2013/04/24 David
if external EEPROM no use (use EC or BIOS),
un-mount R655/R645, mount R899/R646

MODE_CFG1 R5617 1 (R) 2 4K7R2J-2-GP
R5618 1 2 4K7R2J-2-GP
3D3V_EDP_VDDIO

3.3-V R11 4.7KΩ/NC MODE_CFG0
3.3-V R12 4.7KΩ/NC MODE_CFG1
R16 4.7KΩ/NC
R17 4.7KΩ/NC

RTD2136 Supports three operation mode for system design.
Reserved 4.7K resistor pull up/low for mode selection

ROM ONLY Mode : PIN47 4.7K pull low, PIN48 4.7K pull high
EP Mode : PIN47 4.7K pull high, PIN48 4.7K pull low
EEPROM Mode : PIN47 4.7K pull high, PIN48 4.7K pull high

PS8625_BKLT_PWM R5619 2 100KR2J-1-GP (63.10434.1DL) DP_VARY_BL_R
PS8625_LCD_PW_EN R5622 2 100KR2J-1-GP (63.10434.1DL) PS8625_BKLT_EN

2015/05/12 Jurly
Mount R626/R627R634,Vendor advised

eDP to dual channel LVDS

2012/11/07
Change from PS8625 to RTD2136R Kenyon
Copy from ROSA PBAIO
RTK RTD2136R/71.02136.B03

1D2V_EDP
3D3V_EDP_VDDIO
1D2V_EDP_SWR
R5627 1 2 1KR2J-1-GP
Damon 0309

un-Plug: Low
Plug: High
eDP_HPD_CPU
Damon SA Modify 10/29

PS8625_HPD_R
TEST_MODE
DP_REXT
1D2V_EDP_SWR
PS8625_BKLT_EN
PS8625_BKLT_PWM
DP_VARY_BL_R
EC_SMB_SCL_TSMT
EC_SMB_SDA_TSMT
TSMT_SMB_SCL_U_R
TSMT_SMB_SDA_U_R
eDP_AUX_CON_P
eDP_AUX_CON_N
eDP_TX_C_P0
eDP_TX_C_N0
eDP_TX_C_P1
eDP_TX_C_N1

LVDS_TXE_PC ... LVDS_TXE_N3
LVDS_TXO_PC ... LVDS_TXO_N3
MODE_CFG0
MODE_CFG1

TSMT1 change to 071.02136.0003
Damon SA Modify 11/20

Dual Mode Regulator Configuration

3D3V_EDP_VDDIO
2012/10/14 David
reserved slave address 0x94 & 0x6A
2015/05/23 Jurly del PH
2018/10/20 Damon Wei SA Modify
R5608 1 (R) 0R21-2-GP
R5625 2 0R0402-PAD-2-GP
Form CPU
CPU_SMB_SCL
CPU_SMB_SDA
Form EC
EC_SMB_SCL
EC_SMB_SDA
EC_SMB_SCL_TSMT
EC_SMB_SDA_TSMT
Damon 0410

2012/10/24 David
Reserve the EEPROM (72.24C64.E01) for SA usage.
Once the panel is work normally, can remove EEPROM, and transfer the initial job to EC
2013/04/24 David
R614 Un-mount R655 if external EEPROM no use
R615 4K7R2J-2-GP
TSMT_SMB_SCL_U_R
TSMT_SMB_SDA_U_R

Change to 72.24C64.K01
Damon SA Modify 12/04

EEPROM Mode
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.
1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

3.3-V
U2
MICSDA
MICSCL
SDVCC WP
SDA A2
SCL A1
GND A0
24C128 (SMD)
I2C address=0xA8

EP Mode
External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used

EC
3.3-V R13 4.7kΩ
CICSDA EC_SDA
R15 4.7kΩ
CICSCL EC_SCL

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (RSVD)
Size: Custom | Document Number: Eiffel-2 | Rev: -1
Date: Thursday, June 27, 2019 | Sheet 56 of 106

HDMI V1.4b

HDMI_DDI_TX_P0
HDMI_DDI_TX_N0
HDMI_DDI_TX_P1
HDMI_DDI_TX_N1
HDMI_DDI_TX_P2
HDMI_DDI_TX_N2
HDMI_DDI_TX_P3
HDMI_DDI_TX_N3

C5709 SCD1U16V2KX-3GP

5V_S0

U3/HDMI/DVI TVS suggestion part
1st :075.01043.0073 Amazing
2nd :75.00808.073 AOS
3rd :075.00550.0071 Liteonsemi

R5711
180R2J-1-GP

R5712
180R2J-1-GP

U2/LAN/DMIC TVS suggestion part
1st :075.09904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

use 5V_DDC_HDMI
To prevent leakage

HDMI DDC Level Shift

D5701 change from 75.00056.D7D to 75.00056.07D,
because OBS.Damon SA Modify 11/15

5V_S0
3D3V_S0
3D3V_S0

R5721
2K2R2J-2-GP

HDMI_SCL_CPU
HDMI_SDA_CPU

Follow Eiffel215i-2 KBLU
Damon SA Modify 10/31

Damon 0310

5V_HDMI
5V_S0

Change HDMI1 Symbol from 62.10078.521 to 062.10012.0401
Damon SA Modify 2018/10/25

HDMI HPD

3D3V_S0
3D3V_S0

HDMI cable
un-Plug: Low
Plug: High

un-Plug: Low
Plug: High

HDMI_DET_CPU

2017/04/19
R5710 chagne to short pad

Follow Eiffel215i_KbluDamon SA Modify 10/29

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (HDMI/Conn)

Size: A2 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 57 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (HDMI Power)**

Size	Document Number	Rev
A4	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 58 of 106

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<Variant Name>

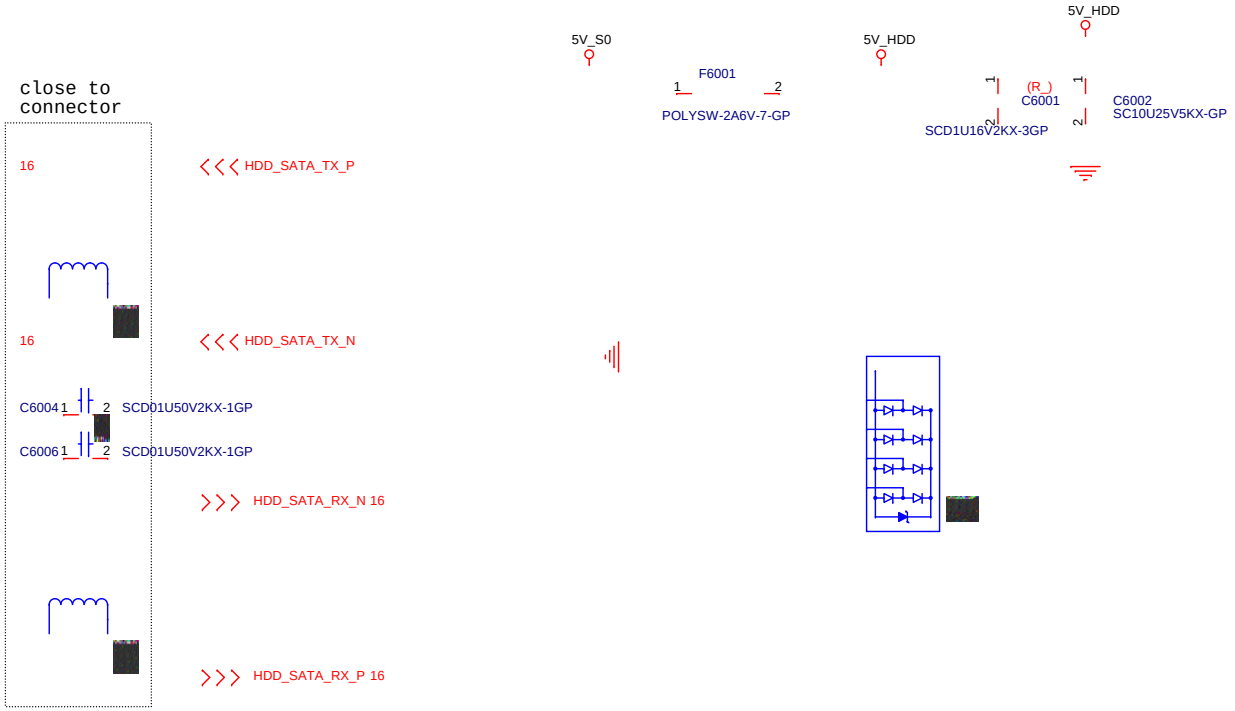
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Display (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 59 of 106	

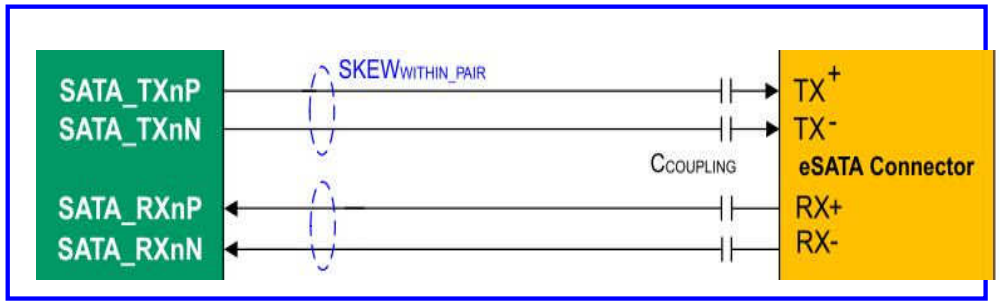
SATA HDD Connector

Layout: Put them together

close to connector



2017/08/14 Damon Wei Modify
SATA1 change F7 from (022.10019.0061) to (022.10019.0021)



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***INT IO (HDD)***	
Size: B	Document Number: **Eiffel-2**	Rev: **-1**
Date: Thursday, June 27, 2019	Sheet 60 of 106	

M.2 2230 / 1630 Key E Type

Mini PCIE (wLAN)

BT_USB20_P
BT_USB20_N

PCIEX1

WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_N_C
WLAN_PCIE_TX_P_C
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P

OTHERS

CPU_SMB_SDA
CPU_SMB_SCL

CNVI

CNV_WR_DN0
CNV_WR_DP0
CNV_WR_DN1
CNV_WR_DP1
CNV_WT_DN0
CNV_WT_DP0
CNV_WT_DN1
CNV_WT_DP1
CNV_WR_CLK_DN
CNV_WR_CLK_DP
CNV_WT_CLK_DN
CNV_WT_CLK_DP
BT_PCMFRM_RSTN
BT_PCMOUT_CLKREQ0
CNV_BRI_RSP
CNV_RGI_DT
CNV_RGI_RSP
CNV_BRI_DT

3D3V_S5
1D8V_S5

WIFI_DISABLE_N
BT_DISABLE_N
PLT_WLAN_RST#
SUS_CLK_CPU

C6103 SC10P50V2JN-4GP (R_)
R6120 100KR2F-L2-GP (R_)

PULSAR_38P4M_REFCLK

2014/10/1-Corree
Change to Key.E
type

062.10003.0611

Close to Pin2/4/72/74

C6108 SC010U6D3VKX-0GP (R_)
C6105 SCD1U25V2KX-0GP
C6107 SCD1U25V2KX-0GP

Add C6108 C6109
Damon SA Modify 11/17

R6105 0R0402-PAD-2-GP
R6107 0R0402-PAD-2-GP
R6110 0R0402-PAD-2-GP
Damon 0419

PCIE_WAKE#
WLAN_CLKREQ_CPU#

2014/10/7
TX connect to TX, RX connect to RX due to symbol error
WLAN Module /KINGSTON,LITE-ON
Pin35 / Pin37 : PCIE_RXP / PCIE_RXN
Pin41 / Pin43: PCIE_TXP / PCIE_TXN

U2/LAN/DMIC TVS suggestion part
1st :075.09904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

2017/09/23 Add TVS Damon Wei SA Modify

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (HDD)
Size: C
Document Number: Eiffel-2
Rev: -1
Date: Thursday, June 27, 2019
Sheet 61 of 106

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*INT IO (RSVD)*	
Size: A4	Document Number: Eiffel-2	Rev: -1
Date: Thursday, June 27, 2019	Sheet 62 of 106	

M.2 SSD

HPGP_M2_SATA_DET#	Module Type
0	SSD-SATA
1	SSD-PCIE

SSD1_PCIE_TX_P0
SSD1_PCIE_TX_N0
SSD1_PCIE_RX_N0
SSD1_PCIE_RX_P0
SSD1_PCIE_TX_P1
SSD1_PCIE_TX_N1
SSD1_PCIE_RX_P1
SSD1_PCIE_RX_N1
SSD1_PCIE_TX_P2
SSD1_PCIE_TX_N2
SSD1_PCIE_RX_P2
SSD1_PCIE_RX_N2
SSD1_PCIE_TX_P3
SSD1_PCIE_TX_N3
SSD1_PCIE_RX_P3
SSD1_PCIE_RX_N3
HPGP_M2_SATA_DET#

PCIE_WAKE#
SSD1_CLKREQ_CPU_N
PLTRST_SSD

SUS_CLK_CPU
DEVSLP2

Damon 0410
R6303 0R0402-PAD-2-GP
R6320 (R_) 0R2J-2-GP

3D3V_S0

RSVD for EMI

M.2 Key M Type

2017/02/28
NGFFB1 change to NGFFM1and add F7 062.10003.0711

H:PCIE
L:SATA

Damon 0410
R6313 0R0402-PAD-2-GP
SSD1_CLK_CPU_P
SSD1_CLK_CPU_N
C6307 SCD22U10V2KX-L1-GP (78.22423.5FL)
C6310 SCD22U10V2KX-L1-GP (78.22423.5FL)

Add to PCIEx4, support x4 Optane
Damon SA Modify 2018/10/25

Change NGFFM1 CONN to 062.10003.0701, follow CE advice
Damon Wei SA Modify 2018/12/07

CLOSE TO PINS 70, 72, 74

C6345 SCD1U16V2KX-3GP
C6304 SC10U6D3V3MX-GP

2017/03/14
C6304//C6307 change symbol from 78.10623.51L(10V) to 78.10622.51L(25V)
Use Common part

CLOSE TO PINS 2,4,12,14,16,18

C6341 SCD1U16V2KX-3GP
C6342 SC10U6D3V3MX-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD-NGFF-1)
Size: C
Document Number: Eiffel-2
Rev: -1
Date: Thursday, June 27, 2019
Sheet 63 of 106

PWRBIN

5V_S5

5V_S0

2012/12/14 David
customer modified LED brightness
to 100 ohm

0805 size

2015/06/22 R618 change to 100 ohm

2014/03/18 Daniel
customer modified LED brightness
to 300 ohm

2012/10/15 David
Follow Pisa's LED cable(VSO)
LED: LL-309AWM2Y-001

12/6 Derek Change R621 to 150R follow Madrid

0805 size

3D3V_AUX_S5

10mW

24

PWRBTN_IN

5V_S5

3D3V_S5

24

SUSLED_N

11/18 Akuan add dummy EC702/EC703

20140116 EMI ISSUE Daniel mont 1000P

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size	Document Number	Rev
B	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 64 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)

Size: A2 | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 65 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board Conn (USB/AUDIO)*

Size	Document Number	Rev
A3	Eiffel-2	-1

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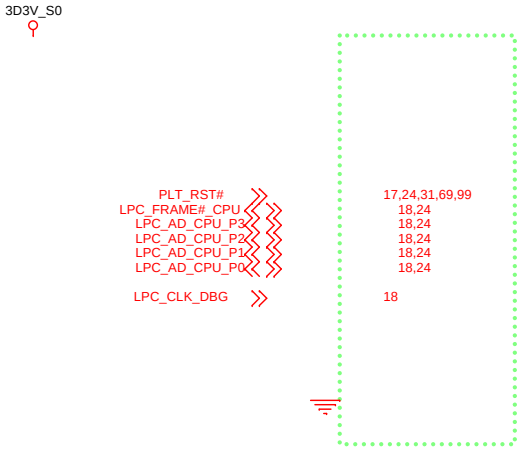
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Sensor (RSVD)***	
Size: A4	Document Number: **Eiffel-2**	Rev: **-1**
Date: Thursday, June 27, 2019	Sheet 67 of 106	

LPC DEBUG PORT

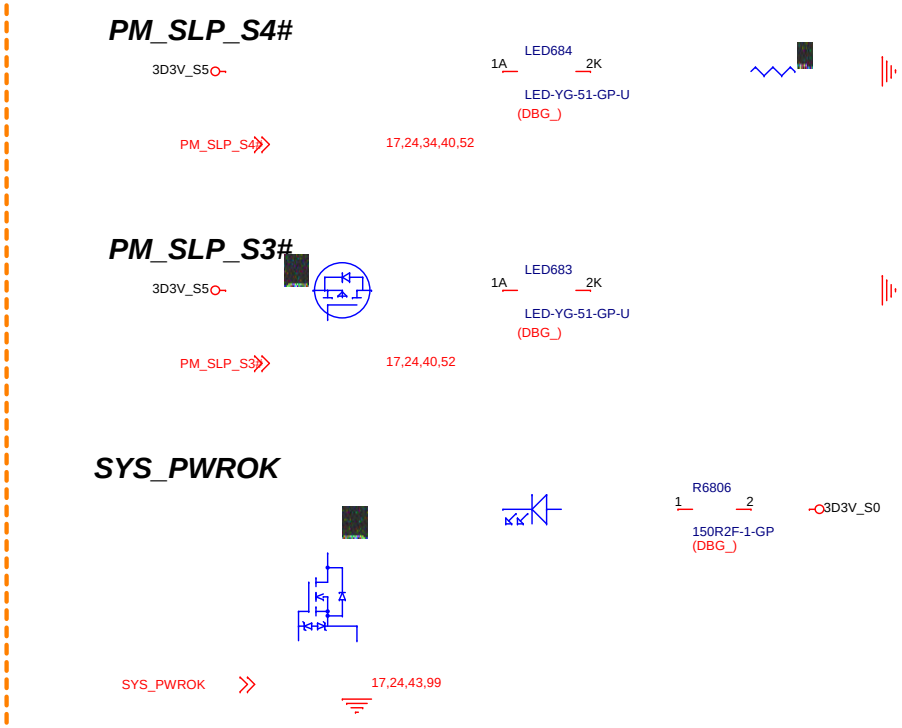


Change DBGH1 from 020.F0522.0010 to 20.F2130.010 ,follow Petra238i
Damon SA Modify 10/26

2017/02/16
change DBGH1 to 020.F0522.0010 Debug header interference. With SSD connector.
2017/10/11 Damon Wei SA Modify Follow Eiffel215i_GLK

Add Debug Led,follow Mocha.
Damon SA Modify 11/17

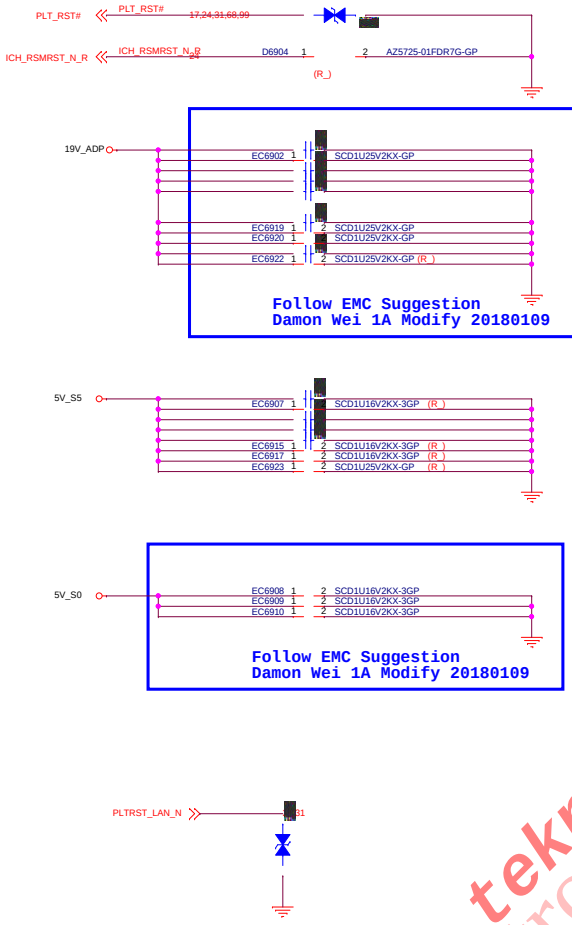
Debug LED



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Debug (LPC debug)	
Size: B	Document Number: Eiffel-2	Rev: -1
Date: Thursday, June 27, 2019	Sheet 68 of 106	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (RSVD)***

Size	Document Number	Rev
C	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 69 of 106

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Sensor (RSVD)***	
Size: A4	Document Number: **Eiffel-2**	Rev: **-1**
Date: Thursday, June 27, 2019	Sheet 70 of 106	

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EXT IO (RSVD)*

Size	Document Number	Rev
A4	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 71 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EXT IO (Type C CC Logic)*

Size	Document Number	Rev
A4	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 72 of 106

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (USB_Type_C)***

Size	Document Number	Rev
A3	**Eiffel-2**	**-1**

Date: Thursday, June 27, 2019 Sheet 73 of 106

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EXT IO (RSVD)*

Size	Document Number	Rev
A4	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 74 of 106

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<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	EXT IO (RSVD)	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 75 of 106	

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (PEG 1/5)***

Size	Document Number	Rev
Custom	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 76 of 106

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (DIGITALOUT 2/5)

Size	Document Number	Rev
Custom	Eiffel-2	-1

Date: Thursday, June 27, 2019 Sheet 77 of 106

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F 3/5)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 78 of 106

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (GPIO/STRAP 4/5)

Size	Document Number	Rev
Custom	Eiffel-2	-1

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (PWR/GND 5/5)***

Size	Document Number	Rev
A2	Eiffel-2	-1

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (VRAM CH AB)**

Size	Document Number	Rev
Custom	Eiffel-2	-1

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<Variant Name>

緯創資通 Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (VRAM POWER)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 82 of 106

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<Variant Name>

緯創資通 Wistron Corporation
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Size: A4	Document Number: Eiffel-2	Rev: -1
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緯創資通 Wistron Corporation
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Title	GPU (RSVD)	
Size A4	Document Number Eiffel-2	Rev -1
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (RT8816A_VGA_CORE)

Size	Document Number	Rev
Custom	Eiffel-2	-1

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (AOZ2262_1D35V_VRAM)

Size: Custom | Document Number: Eiffel-2 | Rev: -1

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<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***GPU (Discharge)***

Size	Document Number	Rev
Custom	**Eiffel-2**	**-1**

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<Variant Name>

緯創資通 Wistron Corporation
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Title	***UNUSED PARTS (RSVD)***	
Size: A4	Document Number: **Eiffel-2**	Rev: **-1**
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WLAN (M2 key E)

HS5
STF256R109H124-GP

1

M.2 Key-M 2280

ME advice change from 334.02D0B.0001 to 334.08002.0001
Damon -1 Modify 06/17

M.2 Key-M 2242

2019/05/08 change from 34.4YP25.201 to 34.4QP10.001

Battery Symbol

23.20068.001
KTS
BBBCR2032BX
23.22063.001 JHT
CR2032 JHT
23.21012.001
KTS
BBBCR2032BN

Scre Hole (PCB New type MOUNTING HOLES)

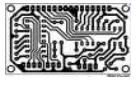
LABEL

MB serial NO# and MAC address
40.3BZ24.011 -> 30 x 15mm
40.3KP03.011 -> 35 x 15mm
45.41107.021 -> 70 x 8mm
40.3BZ23.011 -> 30 x 10mm
40.3BZ24.011 -> 30 x 15mm
CARD
45.ACA01.0C1 -> 32 x 7mm
MIC CARD
345.02801.0001 -> 12 x 6mm

HeatSink Symbol

2016/06/06 Adam change
1st 360.06R02.0001
2nd 360.06R02.0011

PCB Symbol



PCB1
(348.0CW03.00SB)

Part Number	Manufacture (Gerber Out)
348.09008.00SA	CEE (Yes)
348.09009.00SA	HANNSTAR (Yes)
348.09010.00SA	GLOBALBRAN (Yes)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: UNUSED PARTS (RF/EMI)

Size: C | Document Number: Eiffel-2 | Rev: -1

Date: Thursday, June 27, 2019 | Sheet 89 of 106

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<Variant Name>

緯創資通 Wistron Corporation
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Title	*INT IO (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
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緯創資通 Wistron Corporation
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Size: A4	Document Number: Eiffel-2	Rev: -1
Date: Thursday, June 27, 2019	Sheet 91 of 106	

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

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Size: A4 | Document Number: Eiffel-2 | Rev: -1

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緯創資通 Wistron Corporation
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緯創資通 Wistron Corporation
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Title: *EXT IO (RSVD)*

Size	Document Number	Rev
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size A4	Document Number Eiffel-2	Rev -1
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 96 of 106	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Commercial (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
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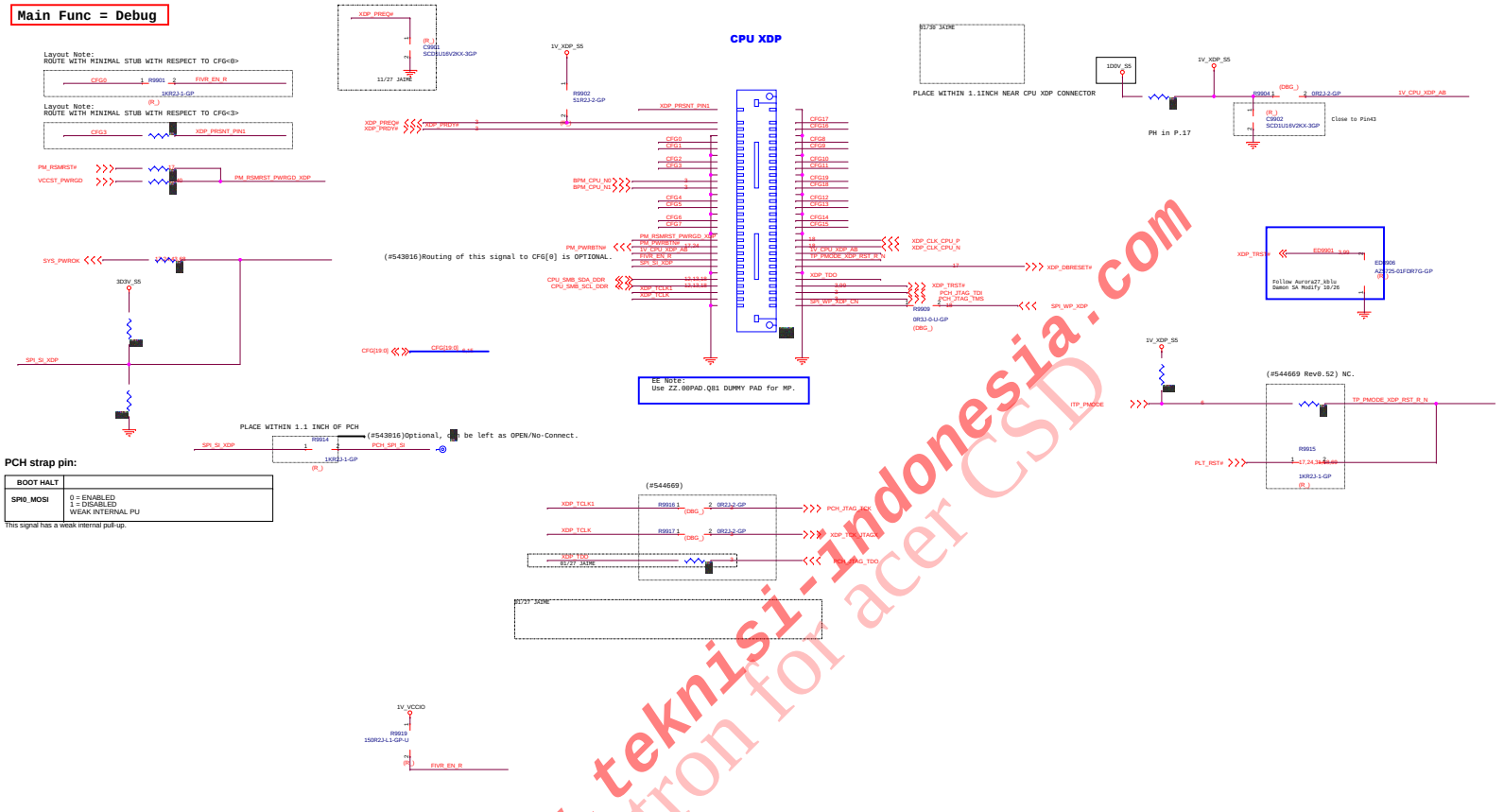
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Commercial (RSVD)*	
Size A4	Document Number Eiffel-2	Rev -1
Date: Thursday, June 27, 2019	Sheet 98 of 106	

Add XDP CONN,follow Aurora27_KBLU
Damon SA Modify 2018/10/25



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Title: Debug (RSVD)

Size	Document Number	Rev
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Table of Content*

Size	Document Number	Rev
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Date: Thursday, June 27, 2019 Sheet 100 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A4	Eiffel-2	-1

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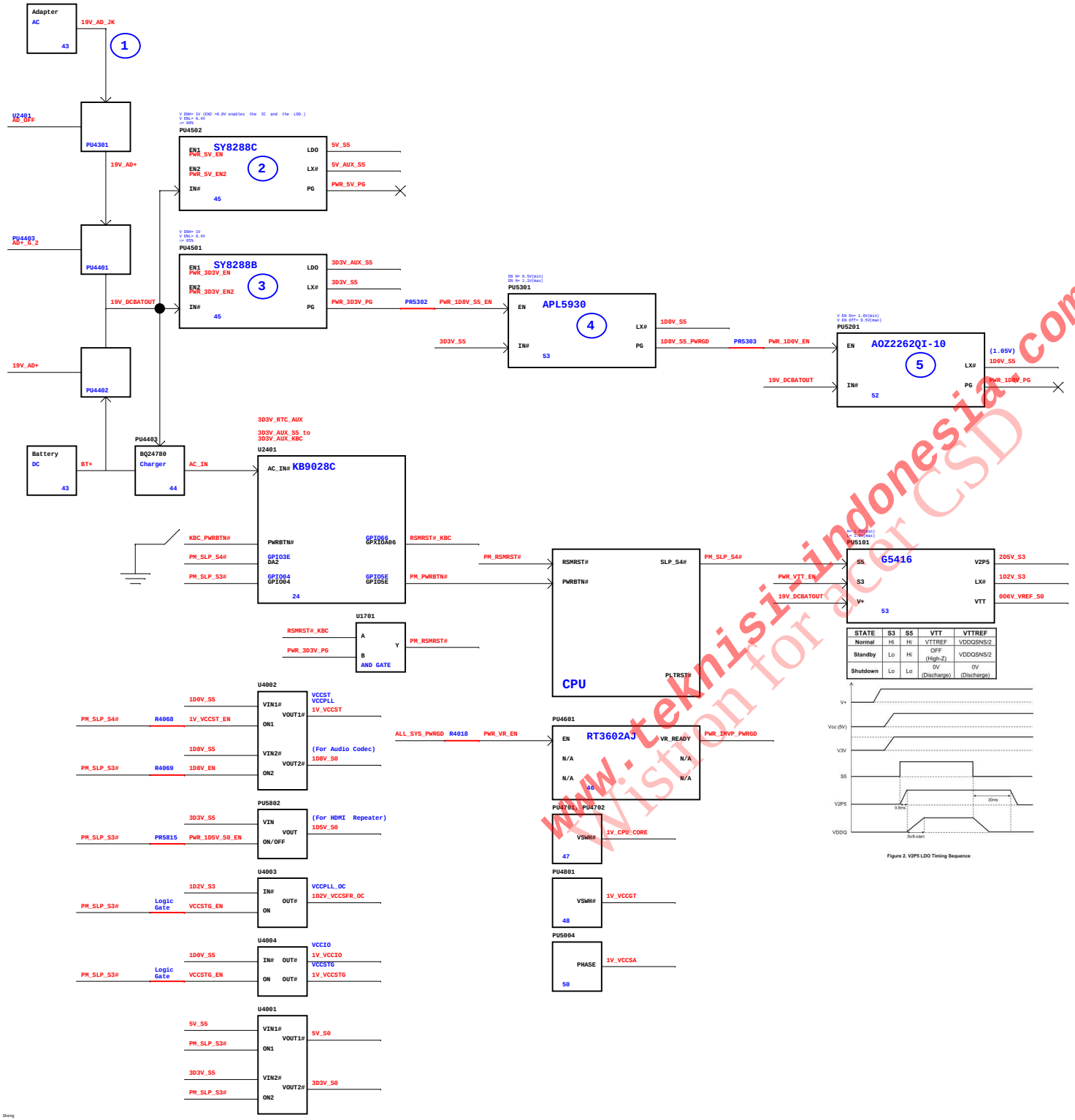
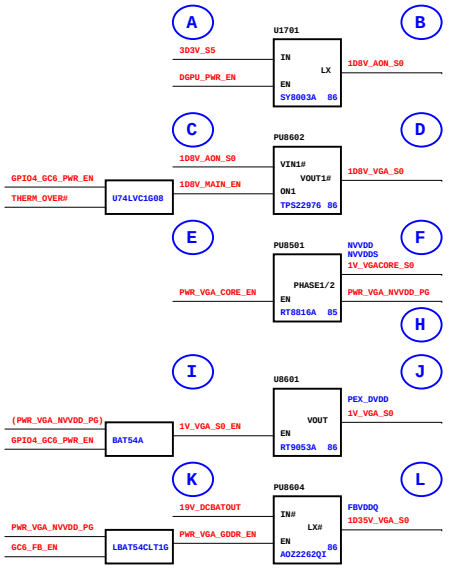




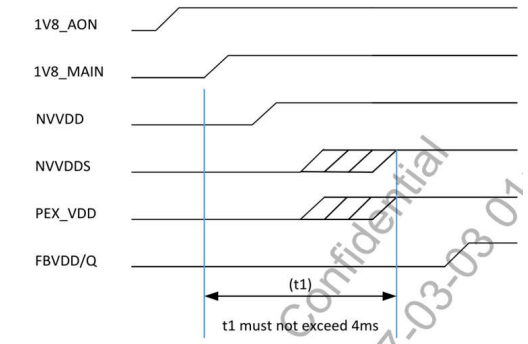


Figure 7.5 Example of Power-Up Sequencing Order

8.2.3 GC6 2.1 Entry/Exit Timing

The following timing diagram in Figure 8.15 and Table 8.2 describes the GC6 2.1 entry and exit sequence and timing requirements.

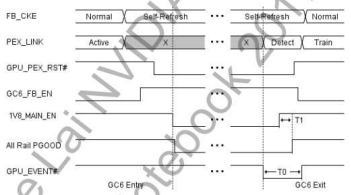
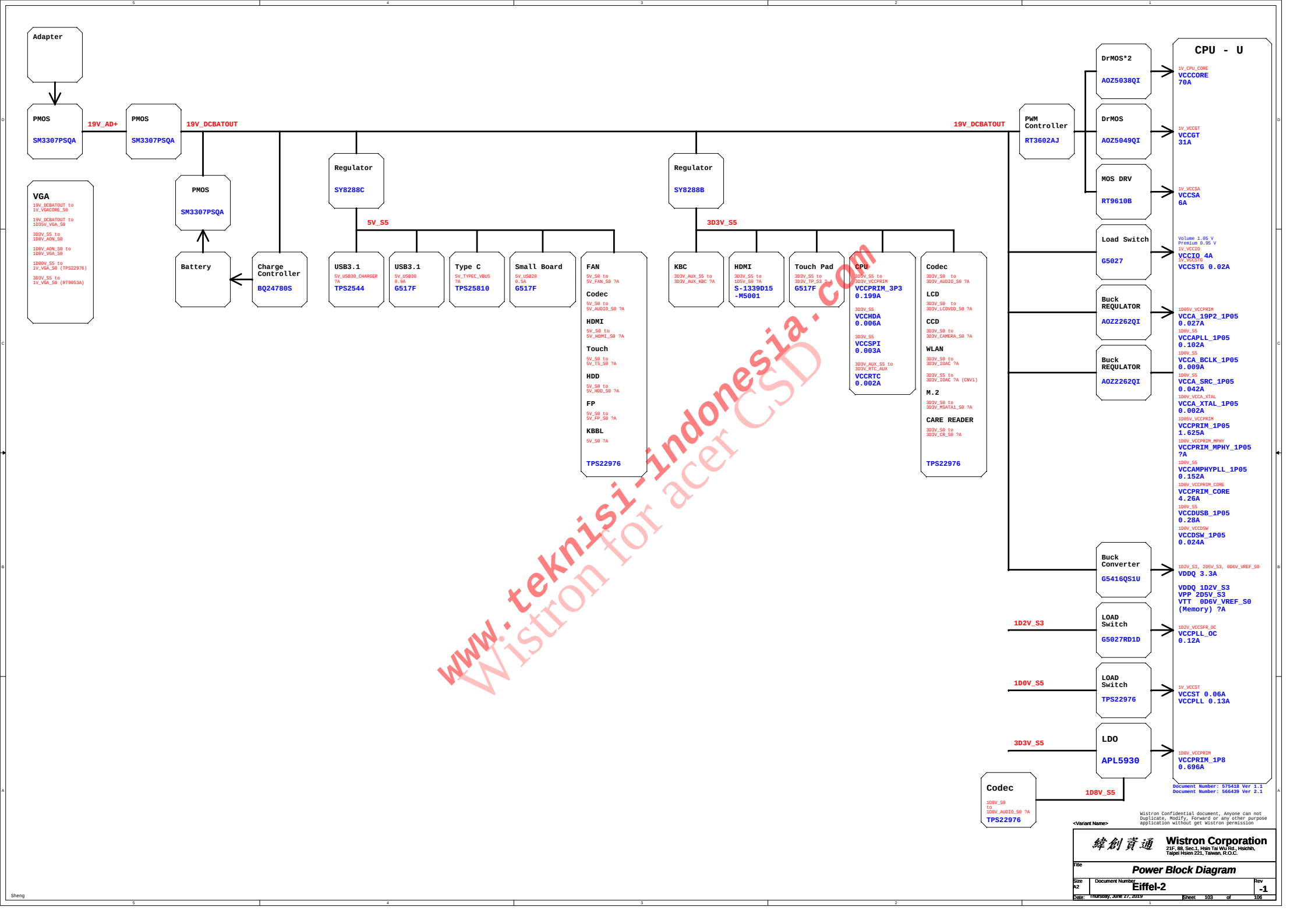


Figure 8.15 GC6 2.1 Entry/Exit Sequence Timing Diagram

Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms


Adapter
PMOS
SM3307PSQA
19V_AD+
PMOS
SM3307PSQA
19V_DCBATOUT
PMOS
SM3307PSQA
Battery
Charge Controller
BQ24780S
VGA
19V_DCBATOUT to 1V_VGACORE_S0
19V_DCBATOUT to 1D35V_VGA_S0
3D3V_S5 to 1D8V_AON_S0
1D8V_AON_S0 to 1D8V_VGA_S0
1D00V_S5 to 1V_VGA_S0 (TPS22976)
3D3V_S5 to 1V_VGA_S0 (RT9053A)
Regulator
SY8288C
5V_S5
USB3.1
5V_USB30_CHARGER ?A
TPS2544
USB3.1
5V_USB30 0.9A
G517F
Type C
5V_TYPEC_VBUS ?A
TPS25810
Small Board
5V_USB20 0.5A
G517F
FAN
5V_S0 to 5V_FAN_S0 ?A
Codec
5V_S0 to 5V_AUDIO_S0 ?A
HDMI
5V_S0 to 5V_HDMI_S0 ?A
Touch
5V_S0 to 5V_TS_S0 ?A
HDD
5V_S0 to 5V_HDD_S0 ?A
FP
5V_S0 to 5V_FP_S0 ?A
KBBL
5V_S0 ?A
TPS22976
Regulator
SY8288B
3D3V_S5
KBC
3D3V_AUX_S5 to 3D3V_AUX_KBC ?A
HDMI
3D3V_S5 to 1D5V_S0 ?A
S-1339D15-M5001
Touch Pad
3D3V_S5 to 3D3V_TP_S3 ?A
G517F
CPU
3D3V_S5 to 3D3V_VCCPRIM
VCCPRIM_3P3 0.199A
3D3V_S5
VCCHDA 0.006A
3D3V_S5
VCCSPI 0.003A
3D3V_AUX_S5 to 3D3V_RTC_AUX
VCCRTC 0.002A
Codec
3D3V_S0 to 3D3V_AUDIO_S0 ?A
LCD
3D3V_S0 to 3D3V_LCDVDD_S0 ?A
CCD
3D3V_S0 to 3D3V_CAMERA_S0 ?A
WLAN
3D3V_S0 to 3D3V_IOAC ?A
3D3V_S5 to 3D3V_IOAC ?A (CNV1)
M.2
3D3V_S0 to 3D3V_MSATA1_S0 ?A
CARE READER
3D3V_S0 to 3D3V_CR_S0 ?A
TPS22976
19V_DCBATOUT
PWM Controller
RT3602AJ
DrMOS*2
AOZ5038QI
DrMOS
AOZ5049QI
MOS DRV
RT9610B
Load Switch
G5027
Buck REQULATOR
AOZ2262QI
Buck REQULATOR
AOZ2262QI
Buck Converter
G5416QS1U
LOAD Switch
G5027RD1D
LOAD Switch
TPS22976
LDO
APL5930
Codec
1D8V_S0 to 1D8V_AUDIO_S0 ?A
TPS22976
1D2V_S3
1D0V_S5
3D3V_S5
1D8V_S5
CPU - U
1V_CPU_CORE
VCCCORE 70A
1V_VCCGT
VCCGT 31A
1V_VCCSA
VCCSA 6A
Volume 1.05 V Premium 0.95 V
1V_VCCIO
VCCIO 4A
1V_VCCSTG
VCCSTG 0.02A
1D05V_VCCPRIM
VCCA_19P2_1P05 0.027A
1D0V_S5
VCCAPLL_1P05 0.102A
1D0V_S5
VCCA_BCLK_1P05 0.009A
1D0V_S5
VCCA_SRC_1P05 0.042A
1D0V_VCCA_XTAL
VCCA_XTAL_1P05 0.002A
1D05V_VCCPRIM
VCCPRIM_1P05 1.625A
1D0V_VCCPRIM_MPHY
VCCPRIM_MPHY_1P05 ?A
1D0V_S5
VCCAMPHYPLL_1P05 0.152A
1D0V_VCCPRIM_CORE
VCCPRIM_CORE 4.26A
1D0V_S5
VCCDUSB_1P05 0.28A
1D0V_VCCDSW
VCCDSW_1P05 0.024A
1D2V_S3, 2D5V_S3, 0D6V_VREF_S0
VDDQ 3.3A
VDDQ_1D2V_S3
VPP 2D5V_S3
VTT 0D6V_VREF_S0 (Memory) ?A
1D2V_VCCSFR_OC
VCCPLL_OC 0.12A
1V_VCCST
VCCST 0.06A
VCCPLL 0.13A
1D8V_VCCPRIM
VCCPRIM_1P8 0.696A
Document Number: 575418 Ver 1.1
Document Number: 566439 Ver 2.1
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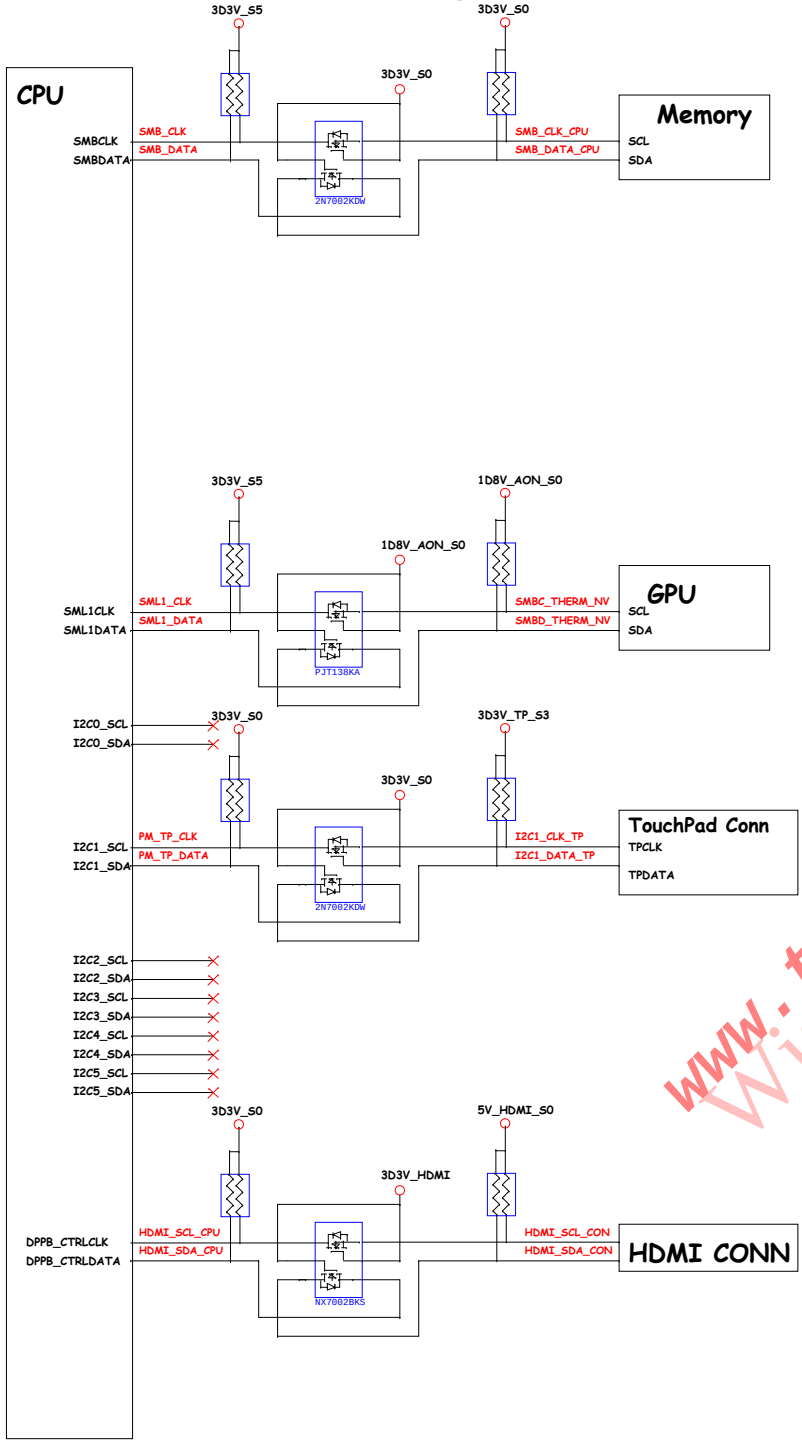
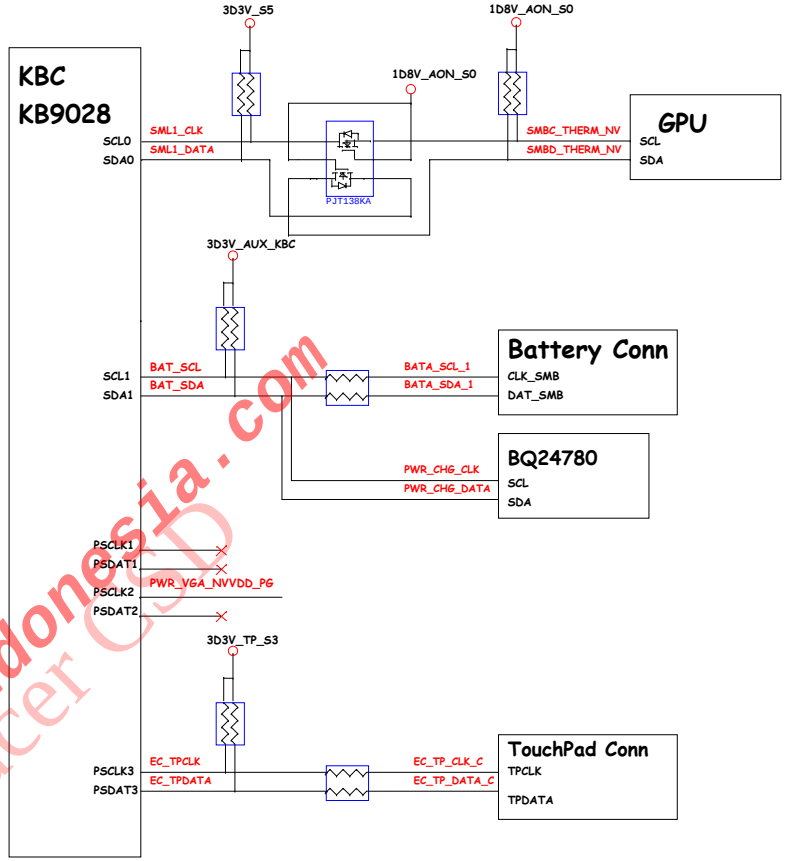
Title
Power Block Diagram
Size A2
Document Number
Eiffel-2
Rev -1
Date: Thursday, June 27, 2019
Sheet 103 of 106
Sheng

SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

Size: A2 | Document Number: Eiffel-2 | Rev: -1

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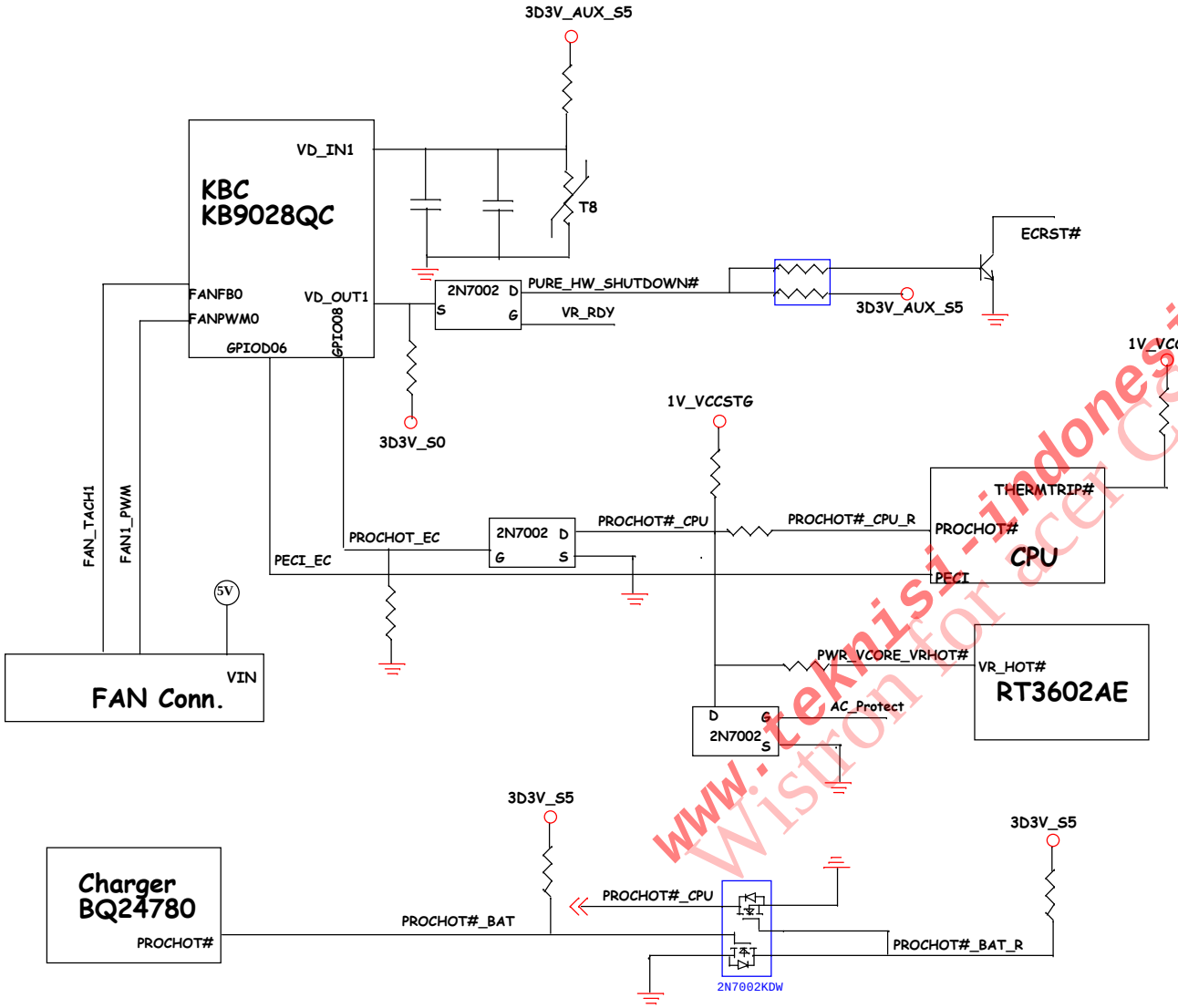
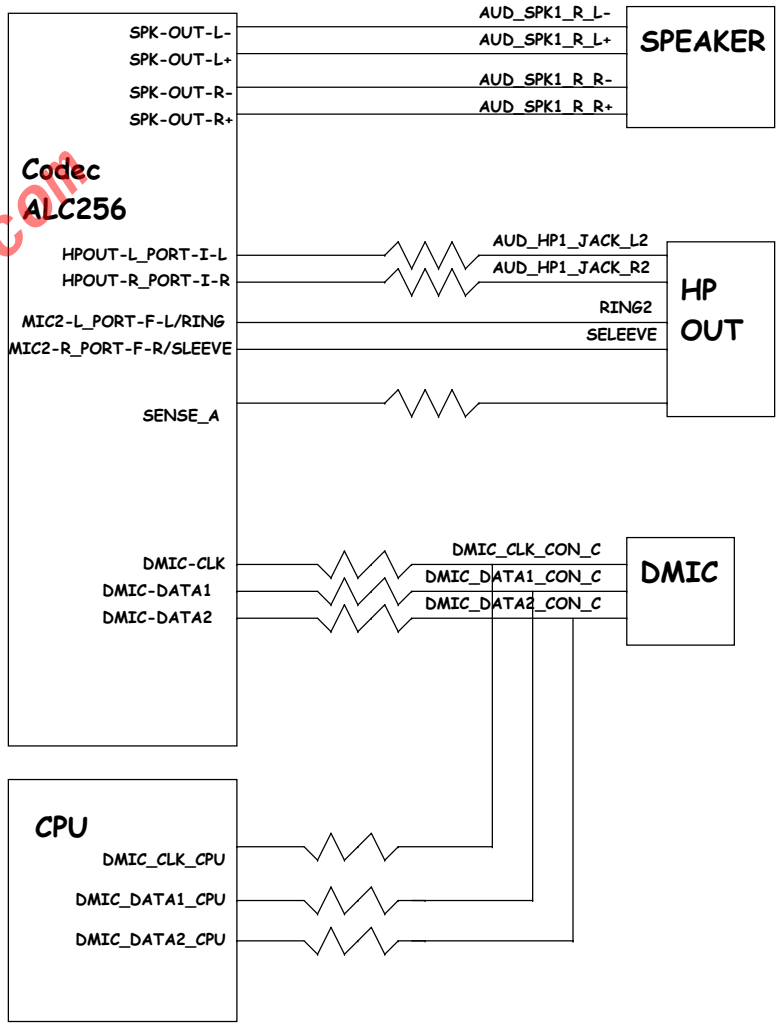
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

Size: A3 | Document Number: Eiffel-2 | Rev: -1

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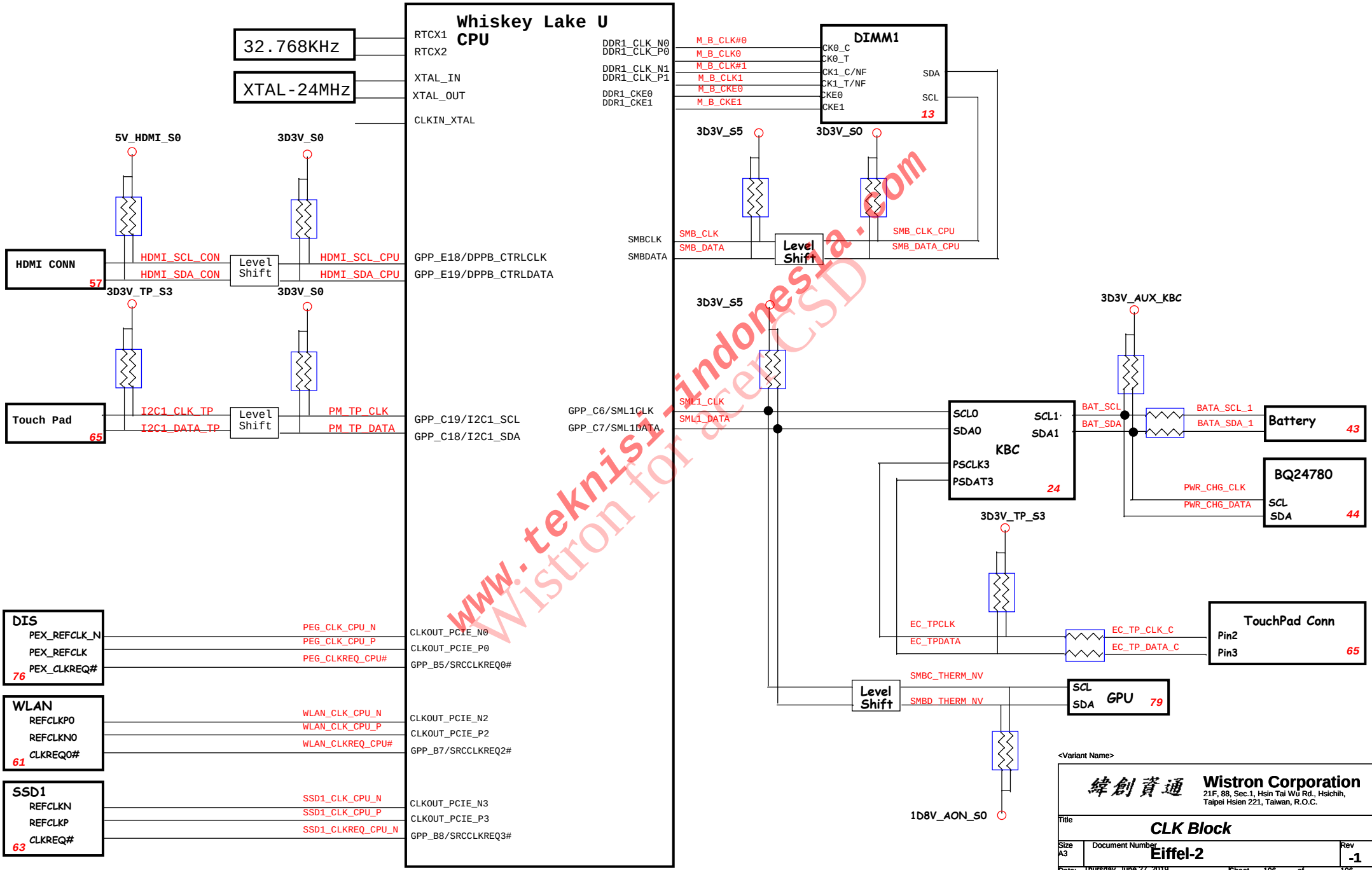
CLOCK BLOCK DIAGRAM



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